FINAL REPORT

RELIABLE LOW-POWER THIN-FILM
SPACECRAFT MEMORY

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

CONTRACT No. NAS5-3171

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UNIVAC

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ABSTRACT

This contract was initiated to develop an engineering model of a Reliable, Low-Power, Thin-Film Spacecraft Memory for the NASA Goddard Space Flight Center. This development was performed under contract number NAS5-3171.

The general characteristics of the memory developed under this contract and projected characteristics of prototypes qualified for satellite and other aerospace applications are given below.

Summary of Engineering Model Characteristics

Memory element	Magnetic, thin-film, plated-wire
Storage capacity	98,304 bits
Speed	100-kilocycle, serial bit rate
Operating mode	Nondestructive readout, serially addressed buffer memory
Normal input d-c voltage	+28 volts, +5.5 volts, and -4.5 volts
Total input power at +25°C	Standby: 0.182 watt including 0.094 watt of loss in d-c to d-c inverter
	Readout: 100 kilocycles continuous 0.434 watt, including 0.134 watt of loss in d-c to d-c inverter
	Write: 100 kilocycles continuous 0.546 watt, including 0.167 watt of loss in d-c to d-c inverter
Operating Temperature Range	-20°C to +50°C
Input Data and Output Data	Serial NRZ bits

binary 0   0 volts to +0.5 volt
binary 1   5 volts to +6 volts

Possible Physical Characteristics
for
Flight Prototypes

100,000-bit buffer memory	145 cubic inches
100-kilocycle serial bit	4 pounds
rate	0.4 watt
2,800,000-bit buffer memory	624 cubic inches
500-kilocycle serial bit	45 pounds
rate	1.5 watts
8192-word, 10 bits/word,	145 cubic inches
random access,	3.8 pounds
10-kilocycle word rate	0.4 watt
8192-word, 20 bits/word,	300 cubic inches
random access,	10 pounds
one-megacycle word rate	15 watts

The estimated volumes and weights for the prototypes are based on the same low-power, discrete-component cordwood circuits used in the engineering model. These numbers can be reduced by the use of thin-film and integrated circuits. At the present time, integrated circuits require more power than the discrete-component or thin-film circuits. Rapid advances in the semi-conductor technology probably will eliminate this one disadvantage of integrated circuits for satellite applications.

FOREWORD

This is the final report on work performed under contract NAS5-3171. This contract with the UNIVAC Division of Sperry Rand Corporation was initiated by Mr. R. Muller, the NASA Goddard Space Flight Center Technical Officer for this contract. The work was performed at the UNIVAC Engineering Center, Blue Bell, Pa., under the supervision of Mr. G. Fedde, who was the project engineer and Supervisor of the Advanced Memory Development Laboratory. Mr. T. H. Bonn, Engineering Manager of the Advanced Components and Circuits Section was responsible for the general management of the contract. Messrs. C. Chong, G. Guttroff, C. Nelson, D. Hanson, F. Hanson, E. Schwartz, and R. Mosenkis, who were engineers in the Advanced Memory Development Laboratory, and G. Reid, A. Schultz, and J. Mueller, who were engineers in the Electronic Components Packaging and Connections Laboratory, worked directly on the project along with many others who made valuable contributions.

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SECTION 1

INTRODUCTION

The design goals of this contract were to develop a reliable thin-film spacecraft memory with a total power consumption of 133 milliwatts. The design requirement was for a power consumption of less than one watt. The engineering model of the memory developed under this contract has 98,304 bits of storage capacity and operates at any bit serial information rate up to 100 kilocycles.

The design approach chosen to achieve the low-power goals was based on the use of magnetic thin-film plated-wire memory elements. These elements were chosen for their small size, nondestructive readout capability, and very fast switching speed. The nondestructive readout permits as many readouts of the stored information as desired without the need for additional power which would be required to regenerate information in a destructive readout memory. The very fast switching speed permits an extremely low duty factor in the drive circuits. The very small size of the memory element reduces the voltage requirement for the drive source and thereby minimizes power consumption.

Discrete components were used in the memory circuit design because they provided maximum design flexibility during the development program and also permitted lower power circuit designs than would have been possible with integrated circuits at that time. Many of the circuits were designed with complementary NPN and PNP transistors connected such that no standby power is used when the circuits are not operated.

Power consumption in the memory system was also minimized during design by handling bits in parallel within the memory. Although the external interface with the memory is bit serial, internal reading and writing operations are in a 16-bit parallel mode. The 16-bit parallel mode was carefully chosen

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to give the minimum power consumption based upon the sense amplifier standby power and the word-drive-circuit pulse power.

The completed memory requires a standby power of 0.182 watt, which includes 0.094 watt of losses in the d-c to d-c inverter. Continuous 100-kilocycle reading requires 0.434 watt, which includes 0.134 watt of losses in the d-c to d-c inverter. There is a 94-percent calculated probability that the memory system will retain 95 percent of its memory capacity in good operating condition for one year. The calculated probability that the memory will retain 100 percent of its capacity is 90.22 percent for one year. These calculations are based on the component failure rates given in Section 2 of this report. These calculations did not include a reliability figure for the memory element because statistically valid reliability figures for the element are not available; but a comparison of the elements used with similar magnetic memory elements makes it very reasonable to expect that thin-film plated-wire elements will be as reliable as ferrite memory cores.

Section 2 of this report gives the details of the memory system design, reliability calculations, the operation of the memory element, the organization of the memory, and the component derating factors that were used in the circuit designs. Section 3 contains detailed reports of the worst-case circuit designs for each of the circuits used in this memory system. Section 4 describes the packaging and explains the techniques that were rejected as well as those that were finally used in the construction of the engineering model. Section 5 gives the detailed results of the acceptance tests held at the UNIVAC Engineering Center on May 27, 1964, and the results of many systems tests to determine the operating margins. Section 6 offers conclusions and recommendations for future development work. The appendices contain all of the detailed logic diagrams, schematics, parts list, and memory layout diagrams.

SECTION 2

MEMORY SYSTEM ORGANIZATION

2.1. THE PLATED-WIRE MEMORY ELEMENT

The memory element consists of a wire substrate which is made of beryllium-copper drawn to a 0.005-mil diameter and which is electroplated with a magnetic thin film. The magnetic film is the same 81-percent nickel, 19-percent iron alloy widely used in planar thin-film memory elements. The coating is continuous and is plated in the presence of a circumferential magnetic field that establishes a magnetic anisotropy axis, or preferred magnetization direction, circumferentially around the wire. Figure 1 is a simplified diagram of the plating apparatus and the electrical test that provides control of the process. The magnetic material is electroplated on a continuously moving wire in room environment. The continuously moving wire is electrically tested with a complete operating memory pulse program.
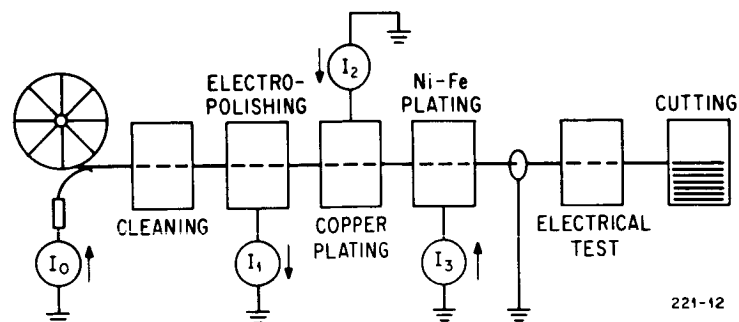
Figure 1. Wire Plater and Tester

The manner in which information is stored on the wire and the details of the read and write operations are shown in Figures 2 and 3.

Information is stored according to the sense of the circumferential magnetization in the portion of the plated wire enveloped by the word

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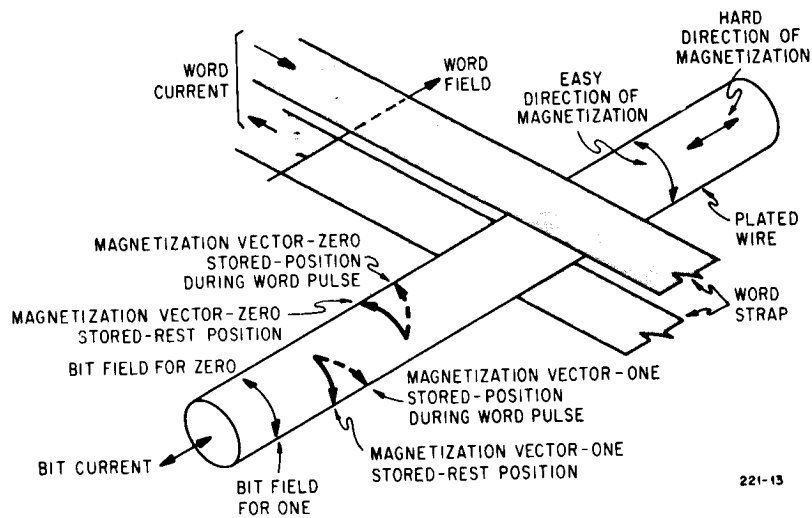
Figure 2. Information Storage on Plated Wire
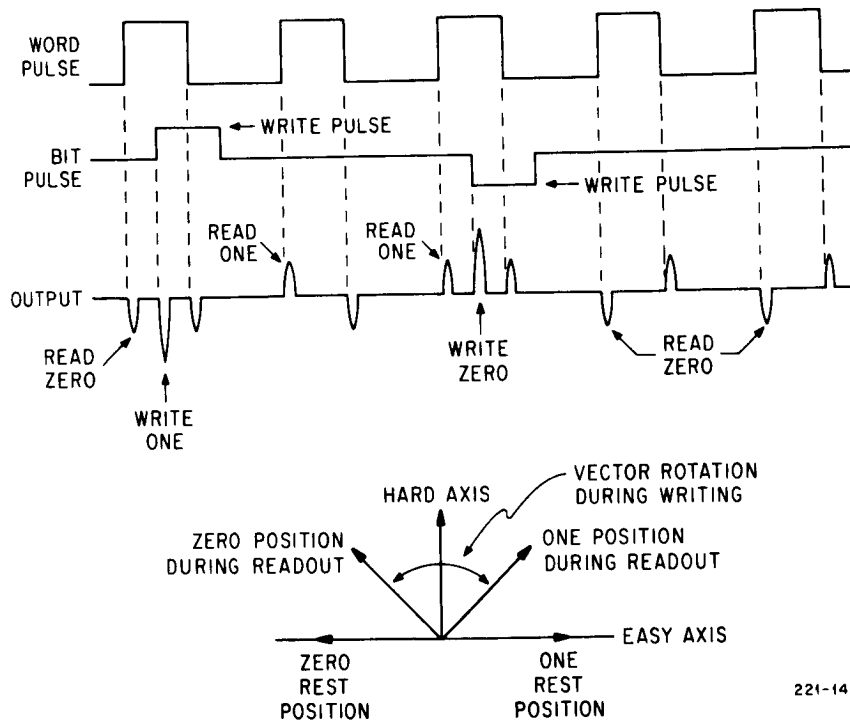
Figure 3. Read and Write Operations

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strap—clockwise magnetization represents a stored 1; counterclockwise magnetization represents a stored 0. To read the stored information, a word current is applied to the word strap which envelops the plated wire at right angles. The word current produces a word field along the axis of the wire. This word field tilts the magnetization vector from its circumferential rest position towards the axis of the wire. The resulting flux change causes a voltage change (sensed at the ends of the plated wire) of one polarity for a stored 1 and of the opposite polarity for a stored 0. The amplitude of the word current is controlled so that when the current is turned off the magnetization vector returns to its original rest position under the influence of the anisotropy and demagnetizing fields; thus, the readout is nondestructive.

Information is written into the wire by the coincidence of the word and steering bit currents through the plated wire. When the bit current flows in one direction, the magnetization vector is so steered that when the bit and word currents are released the vector is in the 1 rest position; when the current flows in the other direction, the vector is in the 0 position.

Typical operating parameters of the plated wire are as follows:

Word-strap width:	35 mils
Word current:	740 milliamperes ±5 percent
Bit currents:	35 milliamperes ±15 percent
Output voltage:	±10 millivolts
Switching time:	≤60 nanoseconds (depending upon word-current rise time)

2.1.L PARAMETER VARIATION

Techniques which improve allowable parameter variation in the plated-wire memory array have been incorporated into the design. By using a double-pulse write technique, an increase in parameter variation is obtained.

If a given storage location has been written 50 times in succession with a 1 then the readout of the first 0 written following the 1's will be 10 to 20 percent lower than if only 0's had been written. This is referred to as history sensitivity and is present in all memory elements in various degrees. This effect is harmful in that it reduces the allowable variations of other

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parameters. Figure 4 shows the presently used technique, which eliminates this history by using a double-pulse write technique. Regardless of the information pattern, every storage location is written with an alternate 1 and 0 pattern. The disadvantage is the extra power required. Further tests have indicated that this technique increases the plated-wire resistance to destructive readout. The drive current amplitude at which destructive readout occurs sets the upper limit on the word drive current. The upper limit was increased by seven percent using this technique because a much shorter word readout current can be used.
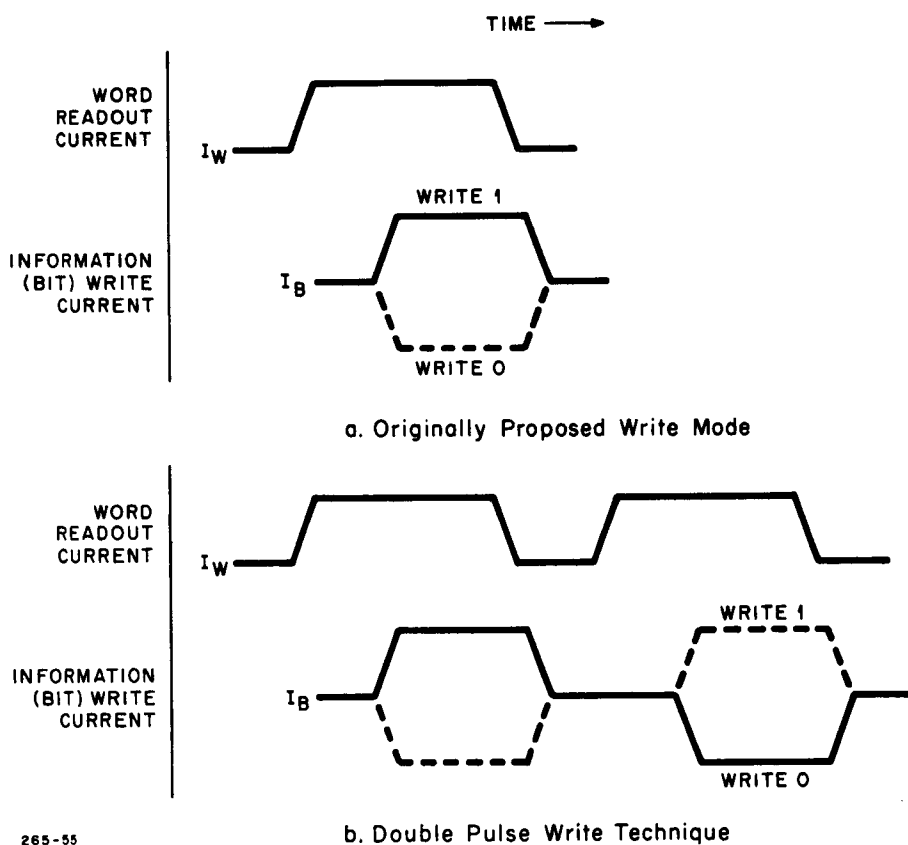
Figure 4. Pulse Technique to Improve
Plated-Wire Performance

2.2. MEMORY SYSTEM ORGANIZATION

The memory model can store 98,304 bits of information. Bits are presented to the memory in one-bit serial fashion. There is no lower limit to the bit rate; the upper limit is 100 kilocycles.

The memory storage elements are contained in a word organized array. The array contains 256 word locations with 192 bits per word. Each word is

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logically subdivided into 12 groups of 16 bits each. The 256 word locations on each side of the array are accessed by means of a 32-by-16 word-selection matrix. Thus, there are $32 \times 16 \times 12 \times 16 = 98,304$ unique memory locations. The general organization of the memory is shown in Figure 5. This organization was used to minimize the power requirement of the memory. Figure 6 is a graph showing the relationship between the power consumption and the number of bits processed in parallel (B). This number is 16 for the memory which was constructed. As can be seen in this graph, the minimum power occurs when B is equal to 30. However, this choice of B equal to 16 requires fewer semiconductors, as will be seen in Figure 7.

Each sense amplifier and associated information register and bit driver consumes a total power of 0.0035 watt. For a given 100-kilocycle information rate, the number of times that the relatively high power word drive circuits must be energized is inversely proportional to B. The pulse energy for this system is approximately 9.384×10^{-4} watt-seconds per cycle.

Figure 7 shows a graph of the number of semiconductors as a function of the number of bits processed in parallel for the total capacity of 98,304. The parameter P in this figure is the number of words on a word line and is 12 for the memory. The choice of B equal to 16 and P equal 12 was a compromise between the conflicting goals of minimum power consumption and a minimum number of semiconductors.

These minima are functions of the circuit designs and the memory size and speed. Emphasis on factors other than very low power will result in other choices for these parameters.

2.2.1 WRITING INTO THE MEMORY

Incoming information is stored in the information register at a rate of up to one bit every ten microseconds. A count of the number of bits that has been stored in the information register is maintained by the information counter; the counter advances each time a bit is written into the register. When the counter has advanced to a count of 16, the 16 bits stored in the register are written into the first word location of the memory array. The memory-write operation does not interfere with the flow of bits because only a very short time is required to write into the memory (see Figure 8). The maximum repetition rate of the memory-write operation is $\frac{100 \text{ Kilocycles}}{16} =$ 6.25 kilocycles.
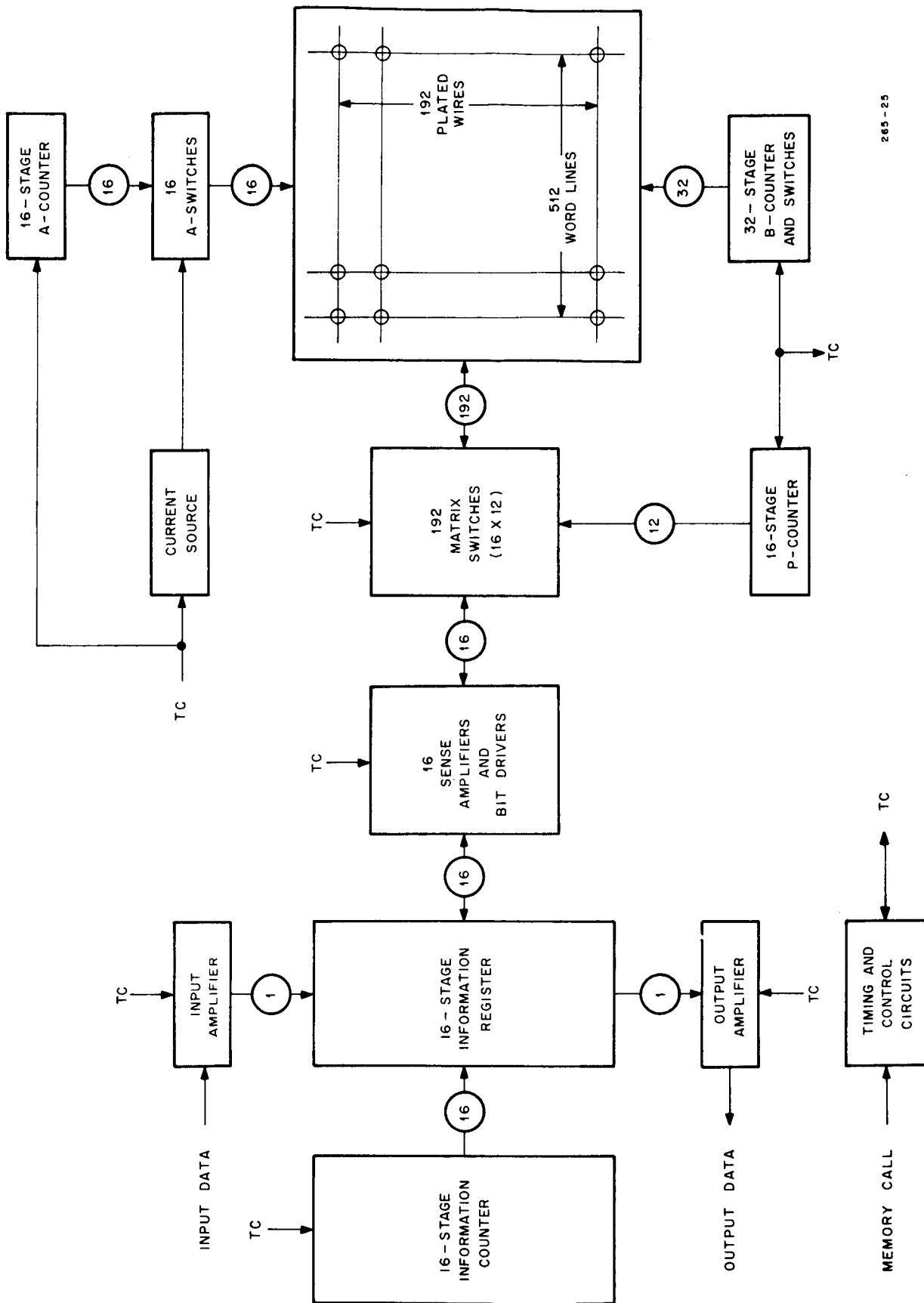
Figure 5. 100,000-Bit Memory, Block Diagram

265-25

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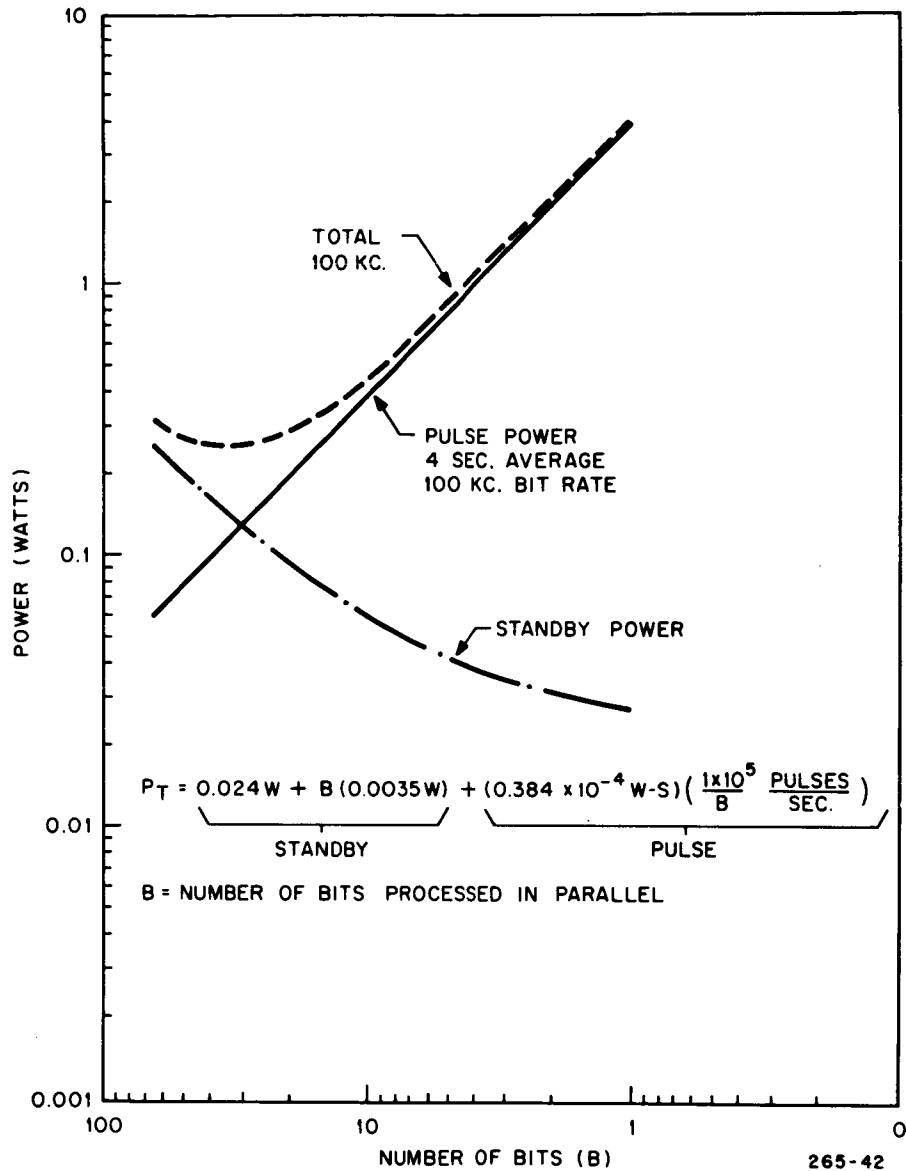
Figure 6. Power Consumption as a Function of the Number
of Bits Processed in Parallel

As previously mentioned, each word location contains 192 bits. There-
fore, the first twelve 16-bit characters are stored in the first word loca-
tion. The characters are counted by a 12-stage ring counter (P-counter)
which drives the 192 low-level switches between the 32 bit drivers and the
192 plated wires. The P-counter advances each time 16 bits are written into
the memory.

When all 192 bit locations of the first word are filled (that is, the
12th stage of the P-counter is set), the next 16 bits are stored in the
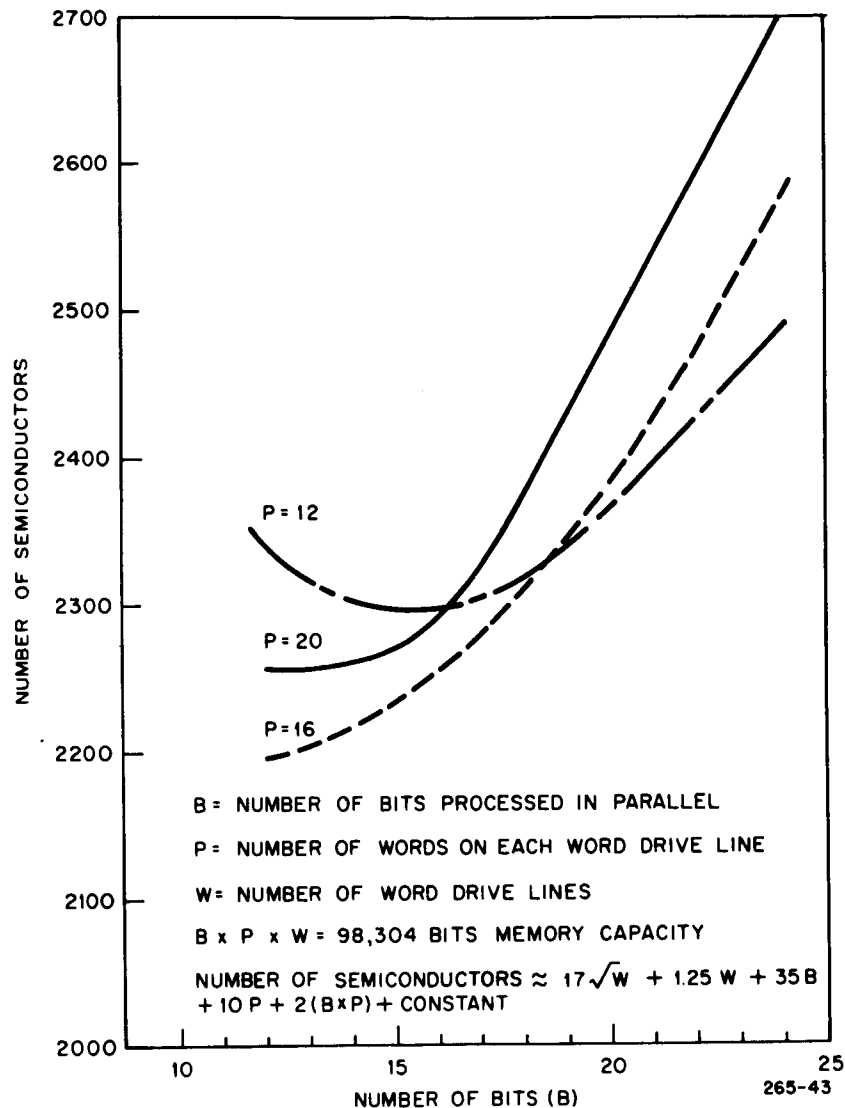
Figure 7. Number of Semiconductors as a Function
of the Number of Bits Processed in Parallel

second word location. The words are accessed by means of a 32-stage B-switch and counter and a 16-stage A-switch and counter. The P-, B-, and A-counters are ring counters, and they are arranged so that each time the P-counter is stepped from 12 to 1, the B-counter is advanced once; and each time the B-counter is stepped from 32 to 1, the A-counter is advanced once. The A- and B-counters and switches cause a current path to be closed through one of 512 word lines, and the P-counter causes 16 current paths to be completed through 16 of the 192 plated wires.

2.2.1.2. READING FROM THE MEMORY. The first clock pulse that occurs during a read instruction causes 16 bits to be read out of the first word location.

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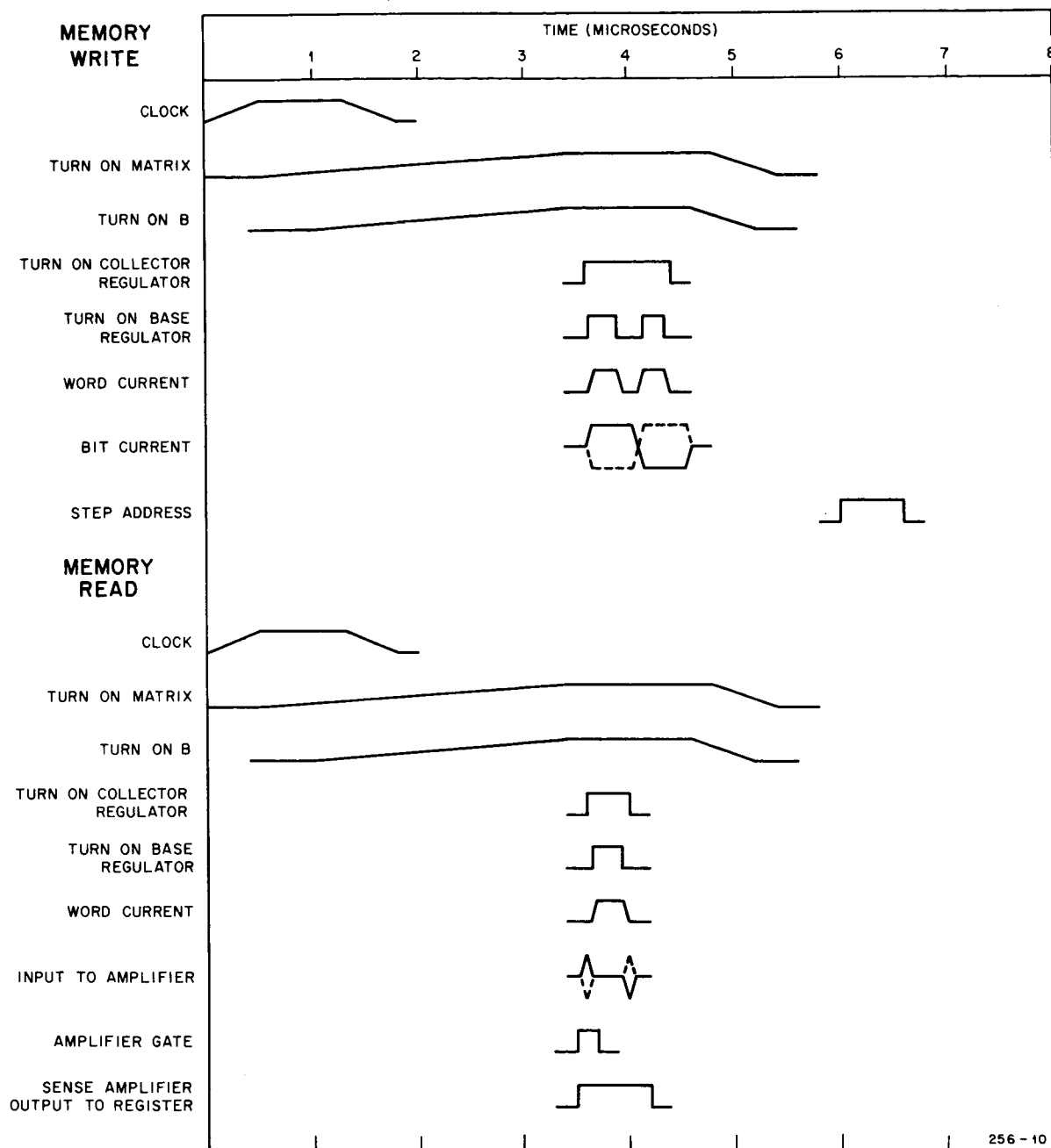
Figure 8. Memory Timing Diagram

These 16 bits are transferred from the plated wires through the low-level matrix switches and sense amplifiers into the information register. When the register is loaded, the first bit is sent out of the memory. The next clock pulse steps the information counter to 2 and causes bit 2 to be sent out, and so on.

Each time 16 bits are read out of the memory, the P-counter advances by a count of one. Each count advance causes the next group of 16 bits to

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be read out of the first word location. The process continues until the P-counter contains a count of 12, which means that 12 × 16 or all 192 bits along one word line have been read out. At this time the P-counter steps from 12 to 1, and the B-counter count advances by one. The next 16 bits are read out of the second word location.

2.3. RELIABILITY CALCULATIONS

Early in the design phase calculations were made for the reliability of the system; taken into account were parallel bit channels and line diode failures causing partial failure of the memory. The percentage of memory capacity lost for one, two, and three failures is shown in Table 1. With this simple configuration the probability of survival of various percentages of the memory was calculated using two sets of component failure rate numbers (see Table 2).

Table 1. Memory Capacity Lost

Logically Serial Circuits		Word-Selection Diode Matrix		16-Bit Channels	
No. of Failures	Capacity Lost	No. of Failures	Capacity Lost	No. of Failures	Capacity Lost
1	100%	1	8.8%	1	6.25%
		2	17.6%	2	12.5%
		3	26.4%	3	18.75%

Table 1 shows the worst possible case. In the word-selection diode matrix and the 16-bit channels, there are possible component failures that have a much smaller effect on the amount of memory capacity lost.

Table 2. Memory Survival Rates

Components	A Failure Rate	B Failure Rate
Transistors	0.010×10^{-6}/hr.	0.050×10^{-6}/hr.
Diodes	0.002×10^{-6}/hr.	0.005×10^{-6}/hr.
Resistors	0.004×10^{-6}/hr.	0.002×10^{-6}/hr.
Cerbric Cap	0.001×10^{-6}/hr.	0.0025×10^{-6}/hr.
Tantalum Cap	0.035×10^{-6}/hr.	0.010×10^{-6}/hr.
Transformers	0.010×10^{-6}/hr.	0.020×10^{-6}/hr.

Using both sets of numbers yielded a probability of survival for 100 percent of the memory of 90.22 percent (A failure rates) and 73.13 percent (B failure rates). Table 3 shows the probability of survival for various percentages of the memory using both sets of failure rates.

Table 3. Probability of Survival for Various Percentages of Memory

Probability of Survival in Percent		Percent of Memory Capacity Operational	Allowable Number of Failures
A	B		
90.22	73.13	100	0
94.02	83.46	93.75	1 failure in 16 channels
94.09	84.15	87.5	1 failure in 16 channels
94.10	84.18	81.25	3 failures in 16 channels
91.03	74.77	91.2	1 failure in word-selection matrix
94.86	85.34	84.95	1 failure each in one bit channel and word-selection matrix

2.4. COMPONENT DERATING

Technical Report No. 238-1, revision A, dated August 1, 1963, which is comprised of a listing of end-of-life (E.O.L.) factors for the specifications of components used in the aerospace memory, is reproduced under this heading.

Component	Specification @ +25°C	End-of-Life Factor
Diode	I_R max	$2^{\Delta T°C/10} \times 10$
	V_{FSS} & V_{FPK} min	0.8 minus 2.5 mv/°C
	V_{FSS} & V_{FPK} max	1.2 minus 2.5 mv/°C
	t_{fr} && t_{rr} min	0.8
	t_{fr} & t_{rr} max	1.2
	BV	0.5 – 25°C to +55°C

Component	Specification @ +25°C	End-of-Life Factor
Diode (cont)	C_{min}	0.8
	C_{max}	1.2
Transistor	h_{FE} min	0.4 (0.66 for temp and 0.6 E.O.L.)
	V_{CE} max	1.3
	I_{CER} max	$2^{\Delta T°C/10} \times 10$
	I_{CEX} max	$2^{\Delta T°C/10} \times 10$
	I_{CES} max	$2^{\Delta T°C/10} \times 10$
	I_{CBO} max	$2^{\Delta T°C/10} \times 10$
	I_{COFF} max	$2^{\Delta T°C/10} \times 20$ measured @ V_{BE} OFF MAX
	V_{BE} off max	0.5 for I_{COFF} max
	V_{EBO}	0.5 for steady state; 0.8 transient
	V_{CEO}	0.5
	V_{CBO}	0.5
	V_{CER}	0.5
	V_{VE} max	1.2 minus 2.5 mv/°C
Resistor	Initial tolerance ±1%	±3%
Capacitor (coupling)	BV Initial tolerance ±5%	0.1 ±7%, ±0.01%/°C
Capacitor (By-pass)	BV Initial Capacitance	0.5 0.5

Noise

Gain through cascaded stages with a noise signal equal to 0.5 normal signal level shall be less than unity under worst-case conditions.

Power Supply

Voltage sequencing shall not be required for circuits

Supply regulation ±2 percent

D-C distribution ±1 percent

Transient   ±2 percent

Circuits shall withstand supply turn-on transient of +25 percent.

Circuits shall not depend on each other to prevent burn up.

SECTION 3

MEMORY CIRCUIT DESIGNS

GENERAL

This section contains detailed descriptions of the memory circuits used in the 100,000-bit memory system. The presentation is subdivided into discussions of four major circuit groups. The logic and control circuits are presented first because of their general use throughout the system. Special circuits which are directly related to the operation of the plated-wire memory are presented in two parts. Power supply circuits are described last.

Each circuit description contains the circuit specifications, a general analysis of its operation, and a detailed explanation of the design procedures used to arrive at an operational circuit. Worst-case calculations and other detailed design information are included.

3.1. LOGIC AND CONTROL CIRCUITS

Most of the logic and control circuits are distributed throughout the memory system for the basic timing and logical functions required during a read or write cycle. The following circuits are discussed under this heading:

    Information Flip-Flop
    Diode AND Gate
    Output Buffer, Flip-Flop, and Driver
    16-Stage Information Ring Counter
    Inverting and Amplifying Circuits
    Delay Flop—Types F and S
    Read/Write Trigger Gate
    Sense Amplifier and Bit-Driver Gate
    High-Power Drivers
    Signal Inverters

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3.1.1. INFORMATION FLIP-FLOP

Specifications

Power Dissipation—approximately one milliwatt per flip-flop

Trigger-Pulse Width—less than 0.2 microsecond at +25°C

Input—may have fan-in of up to 16

3.1.1.1. DESCRIPTION. The information flip-flop consists of two diode/
transistor-logic (DTL) stages interconnected as shown in Figure 9. Points
A and B are normally connected to a positive potential, and either Q1 or Q2
is normally conducting.

Figure 9. Information Flip-Flop

Assume that Q1 is conducting and that Q2 is at cutoff. When a negative-
going input which is less positive than +0.3 volt and which is at least 0.2
microsecond in duration is applied to point B, Q2 conducts and turns Q1 off.
An input at point C which can supply at least 20 microamperes of base current
for 0.2 microsecond to Q2 will also cause Q2 to conduct. The conducting
states of Q1 and Q2 can be reversed by a pulse at point A.

3.1.1.2. DESIGN PROCEDURE. Resistors R1 and R3 were chosen to limit the
power per flip-flop to 1.0 milliwatt. An increase in R1 or R3 to reduce the
power further would result in excessive switching speeds because the turn-off
time depends on the collector RC time constant, where C is stray capacitance.
Diodes D1 and D3 were selected for their high conductance, high speed, and

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low leakage. Diodes D2 and D4 are never reverse-biased in this application; thus, leakage current is unimportant. Low-speed diodes were chosen for D2 and D4 because most of the reverse current that flows through the diodes when they are switched from a high forward current to a low forward current also flows through the base of the transistor. This reverse base current results in a faster turn-off.

Resistors R2 and R4 were chosen so that a maximum of +0.2 volt would be applied to the base-emitter junction of an off transistor at +50°C E.O.L.

3.1.1.3. EQUATIONS OF OPERATION. The collector current of Q1 may be found as follows:

$$I_{C1} = I_L + \frac{V_{CC} - V_{CE1} - V_{d3}}{R1} \tag{1}$$

where I_L is the load current.

The base current of Q1 may be found as

$$I_{B1} = \frac{V_{CC} - V_{BE} - V_{D4}}{R3} - \frac{V_{BE}}{R2} - I_{LK} \tag{2}$$

where I_{LK} is leakage current caused by the input fan-out. The equations for Q1 are identical for Q2.

3.1.1.4. CALCULATIONS. In these worst-case calculations, an underline indicates a minimum value, while an overline denotes a maximum. The tolerance on resistors is taken as ±3 percent E.O.L., and the power supply variation is ±4 percent.

The collector current of Q1 at -20°C and +50°C can be found from equation (1) by using the following values:

I_L = 110 microamperes $V_{CC} = \underline{V_{CC}}$ = 4.8 volts $V_{CE1} = \overline{V_{CE1}}$ = 0.3 volt

$V_{D3} = \underline{V_{D3}}$ = 0.47 volt at -20°C E.O.L. = 0.3 volt at +50°C E.O.L.

R1 = $\underline{R1}$ = 43K

I_{C1} = 370 microamperes at -20°C = 380 microamperes at +50°C

Note that the minimum value of V_{CC} was used, so that I_{C1} calculated here is not $\overline{I_{C1}}$. However, using $\underline{V_{CC}}$ results in a minimum value for I_{B1}.

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This is the more stringent requirement on transistor beta. When solving equation (2) for I_{B1}, the following values apply:

$$V_{CC} = \underline{V}_{CC} = 4.8 \text{ volts} \quad R3 = \overline{R3} = 70K \quad R2 = \underline{R2} = 97K$$

$$V_{BE} = \overline{V_{BE}} = 0.95 \text{ volt at } -20^{\circ}C \text{ E.O.L.} = 0.78 \text{ volt at } +50^{\circ}C \text{ E.O.L.}$$

$$V_{D4} = \overline{V_{D4}} = 1.56 \text{ volts at } -20^{\circ}C \text{ E.O.L.} = 1.22 \text{ volts at } +50^{\circ}C \text{ E.O.L.}$$

I_{LK} = Diode leakage current plus transistor leakage current

Diode leakage current = M(N-1) × leakage current per diode;

Transistor leakage current = M × leakage current per transistor;

where M is the fan-in to the circuit in question and N is the fan-out of each of the M inputs.

Leakage current per diode is 5 nanoamperes at +25°C

Leakage current per transistor is 10 nanoamperes at +25°C

The leakage current at E.O.L. is taken as initial leakage current at +25°C $\times\ 2^{\Delta TOC/10} \times 10$

With M = 1, N = 16 for input, and if M = 1, N = 0 for the other flip-flop transistor:

$$I_{B1} \text{ at } -20^{\circ}C = 59 \text{ microamperes}$$

$$I_{B1} \text{ at } +50^{\circ}C = 71 \text{ microamperes}$$

The required transistor beta is then:

$$\text{at } -20^{\circ}C \quad B = \frac{370}{59} = 6.3$$

$$\text{at } +50^{\circ}C \quad B = \frac{380}{71} = 5.4$$

The minimum hold-off voltage can be calculated at +50°C. The base-emitter junction of the off transistor is slightly forward biased, and the collector leakage current is a strong function of this bias above a certain threshold. This threshold is slightly greater than 0.2 volt.

Minimum hold-off voltage (actually $V_{BE_{OFF}}$ maximum) at $+50^{\circ}C$ (Figure 10) is:

$$\overline{V_A} = \overline{V_{CE1}} + \overline{V_{D1}}$$

where

$\overline{V_{D1}}$ is taken at $I_{C1} = 180$ microamperes

V_{D1} at 70 microamperes $= 0.53$ volt $= 0.57$ at $+50^{\circ}C$ E.O.L.

$\overline{V_A} = 0.3 + 0.57 = 0.87$ volt

assume $i_{OFF} = 7.0$ microamperes or $V_{BE_{OFF}} = +0.21$ volt

with $i_{OFF} = 7.0$ microamperes.

Since $V_A = 0.90$ volt, $V_{R1} = 0.87 - 0.66 = 0.21$ volt

therefore, i_{OFF} must be less than 7 microamperes, thus

$V_{BE_{OFF}}$ maximum is less than $+0.21$ volt.
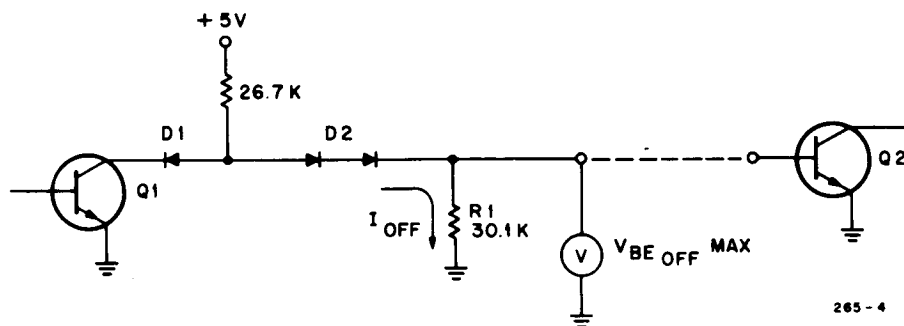
Figure 10. Voltage/Current Analysis of
Information Flip-Flop

3.1.1.5. DEVIATIONS FROM DERATING RULES. None

3.1.1.6. POWER SUPPLY REQUIREMENTS. +5 volt supply

$$I \text{ supply} = \frac{\overline{V}_{CC} - V_{D1} - V_{CE}}{R3} + \frac{V_{CC} - V_{D2} - V_{BE}}{R3}$$

$$= \frac{5.2 - 0.3 - 0.23}{26K} + \frac{5.2 - 0.76 - 0.5}{26K}$$

$$= 180 + 150$$

$$= 330 \text{ microamperes per flip-flop.}$$

3.1.2. DIODE AND GATE

<u>Specifications</u>

a. The AND gate is to deliver at least 23 microamperes into the base of an NPN transistor when all inputs to the gate are at approximately +5 volts (>3 volts).

3.1.2.1 DESCRIPTION. When a pulse with an amplitude of V_1 is applied to resistor R1 (Figure 11), a current i_1 the amplitude of which is close to V_1/R will flow through diode D1 if the inputs to D2, D3, and the other diodes are at $+V_1$. If any input is at ground potential, a current, i_2, will be diverted by that input, and no current will flow through D1.
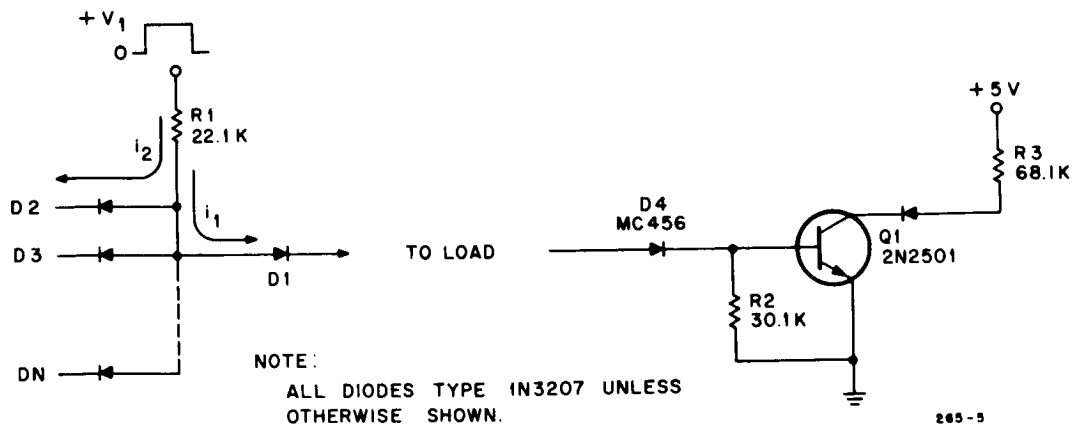
Figure 11. Diode AND Gate

3.1.2.2. DESIGN PROCEDURE. Low-capacitance, fast-reverse-recovery diodes were chosen for D1 for two reasons. The first reason is that 16 gates buff together into the base of one transistor, thus requiring one gate to charge the junction capacitance of D1 in the other 15 gates. The second reason is that D1 feeds the base of a flip-flop transistor in some applications. The $+V_1$ pulse, when applied to R1, causes the flip-flop to set; when the $\pm V_1$ pulse ends, the reverse current that flows through D1 would also flow through the base of the flip-flop transistor and cause the flip-flop to reset prematurely. A fast recovery diode prevents this from occurring.

3.1.2.3. EQUATIONS OF OPERATION. The current i_1 which flows into the base of Q1 through a level shift diode D4 may be found as follows:

$$i_1 = \frac{V_1 - V_{D1} - V_{D4} - V_{BE} - V_{BE}}{R1} - \frac{V_{BE}}{R2} \qquad (3)$$

The current i_2 which is drawn away from the gate when an input is near ground is:

$$i_2 = \frac{V_1 - V_{D2} - V_{In}}{R1} \qquad (4)$$

where V_{IN} is the collector-emitter voltage of an on transistor (+0.3 volt).

3.1.2.4. CALCULATIONS. The minimum value of i_1 at -20°C can be found from equation (3) by using the following values:

$V_1 = \underline{V_1} = 3.75$ volts $V_{D1} = \overline{V_{D1}} = 0.65$ volt

$V_{D4} = \overline{V_{D4}} = 0.78$ volt $V_{BE} = \overline{V_{BE}} = 0.95$ volt

$R1 = \overline{R1} = 22.7K$ $R2 = \underline{R2} = 27K$

$i_1 = 40$ microamperes at -20°C.

With the following values, $\overline{i_2}$ can be found at -20°C from equation (4):

$V_1 = 3.75$ volts $V_{D2} = V_{\underline{D2}} = A7V$

$V_{IN} = 0.3$ volt $R1 = \underline{R1} = 21.3K$

$\overline{i_2} = 140$ microamperes at -20°C.

3.1.3. OUTPUT BUFFER, FLIP-FLIP, AND DRIVER (G)

Specifications

a. Provide an NRZ output which will be at one level for a binary 1 and another level for a 0. The levels are +5 and zero volts, respectively. The output level will be determined by 16 AND gates which are sampled serially. The AND gate outputs are buffered together at the input of the output flip-flop.

b. The driver shall have an output impedance of 5K ohms or less.

3.1.3.1. DESCRIPTION. A positive input current i_1 (Figure 12) causes Q1 to conduct. Transistor Q2 is supplied by Q1 and provides its complement. Transistors Q1 and Q2 each supply an input to a diode AND gate which is also supplied with a gate pulse. The gate pulse is steered to Q3 if Q1 is off and to Q4 if Q2 is off. Transistors Q3 and Q4 are connected as a flip-flop. The input current determines whether the flip-flop is to be set or reset by the gate pulse. If the flip-flop is set (Q4 conducts) an additional pulse to the base of Q4 causes no change in the flip-flop, and an NRZ output results. Transistor Q5 merely amplifies the flip-flop output.

3.1.3.2. DESIGN PROCEDURE. The circuits used have the same configuration as the information flip-flop and the diode AND gate. Speed-up capacitors C_1 and C_2 improve the switching speed of the flip-flop, and the resistor values were chosen to provide an output impedance of 5K ohms.

3.1.3.3. EQUATIONS OF OPERATION. Same as equations for information flip-flop and diode AND gate.

3.1.3.4. CALCULATIONS. Values for I_B and I_C for Q1 through Q5 are tabulated below. The values listed are at worst-case conditions for d-c beta.

Transistor	I_B at -20°C (in microamperes)	I_C at I_B -20°C (in microamperes)	Required beta
Q1	22	150	6.8
Q2	23	92	4.0
Q3	40 through D2	92	2.3
Q3	38 through D5	92	2.4
Q4	40 through D4	278	7.0
Q4	38 through D7	278	7.3
Q5	145	930	6.4

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Figure 12. Output Buffer, Flip-Flop, and Driver
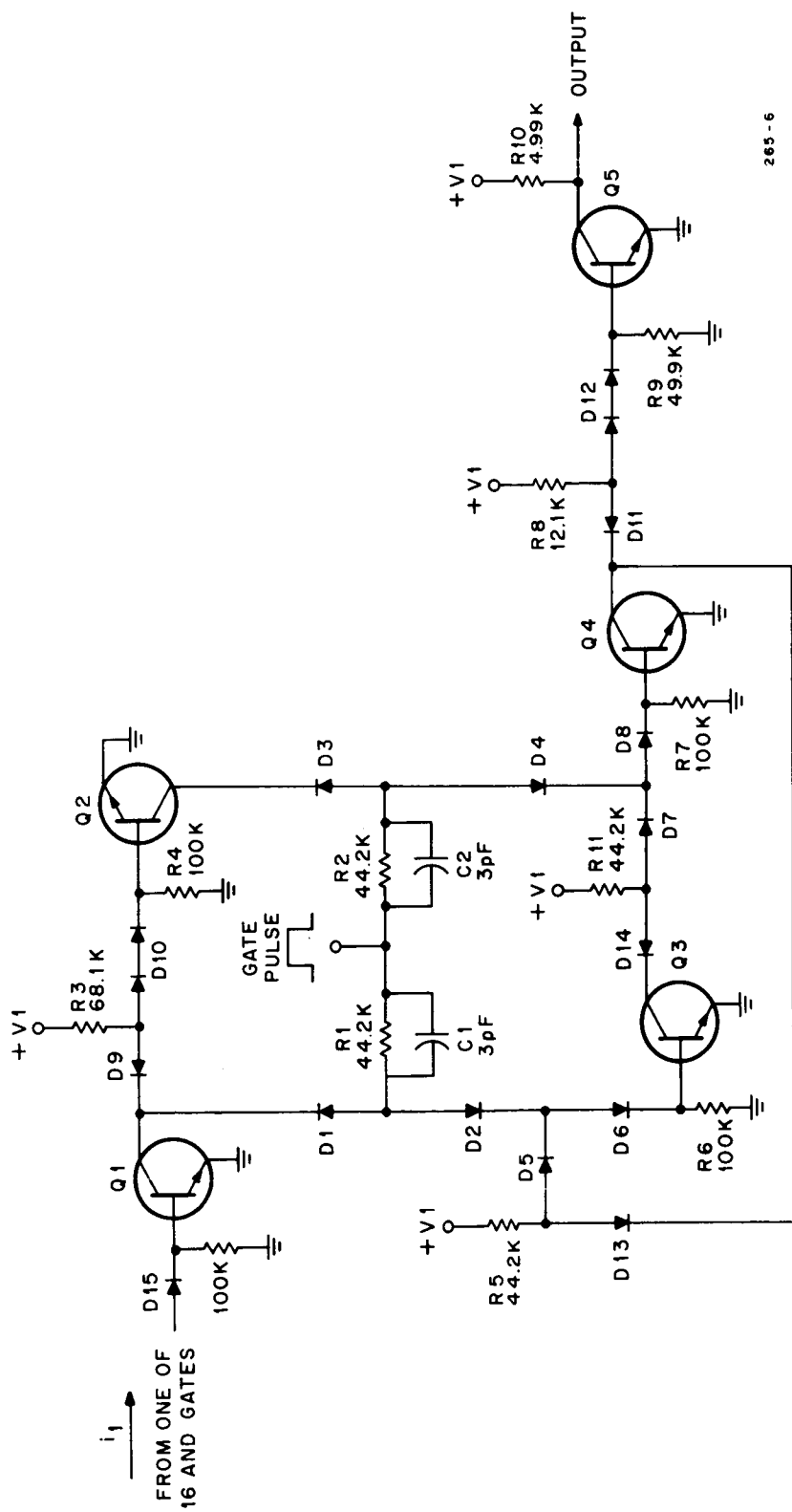
NOTE:
ALL TRANSISTORS TYPE 2N2501.
DIODES (D5,6,7,8,10,12 AND 15) ARE TYPE MC 456
ALL OTHERS ARE TYPE 1N3207.

265-6

The maximum current drawn from the gate pulse at -20°C is:

amplitude of gate pulse $V_G = \overline{V_G} = 4.7$ volts

R1 = R1 = 43K   R2 = R2 = 43K

$V_{D1} = V_{D1} = 0.47$ volt $V_{CE1} = 0.3$ volt

$V_{D4} = V_{D4} = 0.47$ volt $V_{D8} = V_{D8} = 0.56$ volt

$V_{BE} = V_{BE} = 0.67$ volt

Maximum gate pulse current = 80 + 70 = 150 microamperes.

The minimum hold-off voltage is the same as in the information flip-flop.

3.1.3.5. DEVIATIONS FROM DERATING RULES.   None

3.1.3.6. POWER SUPPLY REQUIREMENTS.   +5 volt supply.   The resistors that draw current from the +5 volt supply are listed along with the current drawn at +50°C.   The d-c and pulse power are the same.   Transistors Q2, Q3, and Q5 are conducting; Q1 and Q4 are off.   Voltage V_1 is at +5.2 volts; all resistors are at 97 percent nominal value.

Resistor	Current (in microamperes)
R3	60
R5	92
R8	294
R10	1000
R11	107
Total	1553

3.1.4. 16-STAGE INFORMATION RING COUNTER

Specifications

a. Power dissipation—approximately 10 milliwatts independent of duty cycle.

b. Step pulse amplitude—5 volts, one to two microseconds in duration.

c. Maximum repetition rate—125 kilocycles.

d. Supply 0.75 milliampere to load.

3.1.4.1. DESCRIPTION.   Each stage consists of two complementary transistors which are interconnected to form a flip-flop (Figure 13).
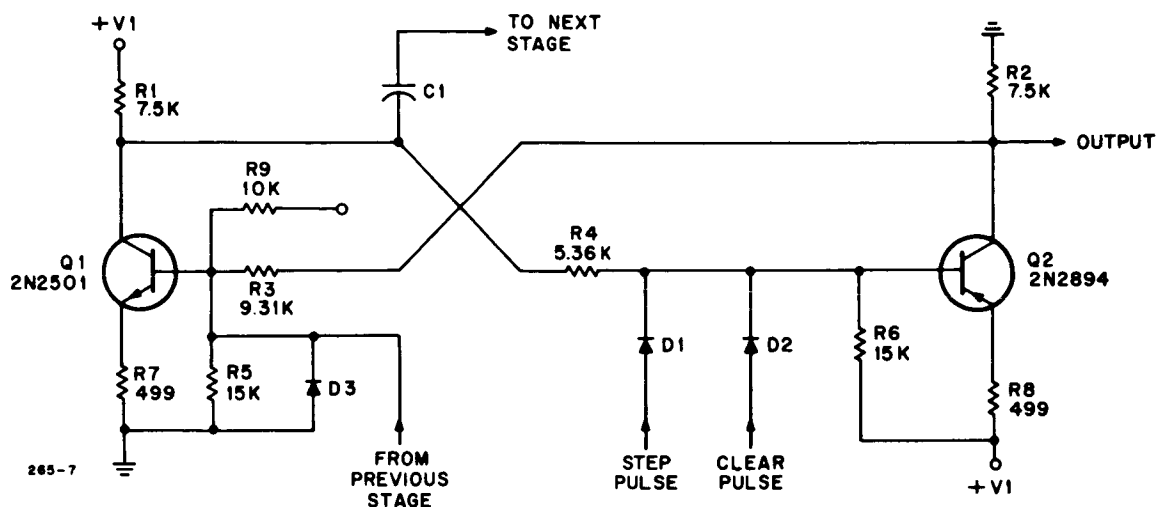
Figure 13. 16-Stage Information Ring Counter Flip-Flop

If Q1 and Q2 are conducting and a step pulse is applied to D1, Q1 and Q2 will turn off. This causes a positive voltage step to be developed at the collector of Q1. This voltage is coupled through C_1 to the base of the NPN transistor of the succeeding stage, thus advancing the count by one.

The emitters of all NPN transistors are returned to ground through a common emitter resistor, R7. Similarly, the emitters of all PNP transistors are returned to V_1 through R8. The voltage developed across the common emitter resistor by the ON stage acts as a reverse bias for the other stages. Diode D3 protects the base-emitter junction of Q1 from excessive reverse voltage when C_1 discharges.

3.1.4.2. DESIGN PROCEDURE. Resistor R1 was chosen so that C_1 plus the stray capacity associated with the collector of Q1 would be charged within a specified time (0 to 98 percent in 5 microseconds). The final value of C_1 was the best compromise between short recovery time and triggering stability. This value was determined experimentally. R7 and R8 were chosen large enough to provide good triggering stability but not so large as to provide excessive negative feedback. The optimum step pulse width was found to be 1.5 microseconds experimentally.

3.1.4.3. EQUATIONS OF OPERATION. The collector current of Q1 may be found as follows:

$$I_{C1} = \frac{V_1 - V_{CE1} - I_{e1}R7}{R1} + \frac{V_1 - V_{CE1} - I_{e2}R8 - V_{BE2} - I_eR7}{R4} \qquad (5)$$

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The base current of Q1 may be found as follows:

$$I_{B1} = \frac{V_1 - I_{e2}R8 - V_{BE2} - V_{CE1} - I_{e1}R7}{R3} + \frac{V_{BE1} + I_{e1}R7}{R5} \qquad (6)$$

Similarly for I_{C2} and I_{B2}:

$$I_{C2} = \frac{V_1 - V_{CE2} - I_{e2}R8}{R2} + \frac{V_1 - V_{CE2} - I_{e1}R7 - V_{BE1}}{R3} + I_{LOAD} \qquad (7)$$

$$I_{B2} = \frac{V_1 - I_{e1}R7 - V_{BE1} - V_{CE2} - I_{e2}R8}{R4} - \frac{V_{BE2} + I_{e2}R8}{R6} \qquad (8)$$

3.1.4.4. CALCULATIONS. Assume I_{e1} = 1.0 milliampere and I_{e2} = 2.5 milli-amperes. The collector current and base currents of Q1 and Q2 can then be found at -20°C by using equations (5) through (8) with the following values:

$V_1 = \underline{V}_1$ = 4.8 volts $V_{CE1} = \overline{V_{CE1}}$ = 0.28 volt $V_{CE2} = \overline{V_{CE2}}$ = 0.26 volt

$V_{BE1} = \overline{V_{BE1}}$ = 0.97 volt $V_{BE2} = \overline{V_{BE2}}$ = 1.04 volts $R1 = \underline{R1}$ = 7.3K

$R2 = \underline{R2}$ = 7.3K $R3 = \overline{R3}$ = 9.6K $R4 = \overline{R4}$ = 5.5K

$R5 = \underline{R5}$ = 14.5K $R6 = \underline{R6}$ = 14.5K $R7 = \overline{R7}$ = 515

$R8 = \overline{R8}$ = 515 I_{LOAD} = 1.5 milliampere $R9 = \overline{R9}$ = 10.3K

I_{C1} = 842 microamperes I_{C2} = 2032 microamperes

$\underline{I}_{B1}$ = 74 microamperes $\underline{I}_{B2}$ = 260 microamperes

An input through diode D2 is used to clear a ring counter stage; an input through R9 is used to set the stage.

I_{R9} = 292 microamperes and I_{B1} = 122 microamperes during the clear pulse. Maximum reverse base current at 100°C is one microampere initially for Q2 and 0.01 microampere for Q1. Derating by a factor of ten still allows the base emitter junction to be reverse-biased by 0.5-(10) (10^{-6}) (15) (10^{+3}) volts, or 0.350 volt.

3.1.4.5. DEVIATIONS FROM DERATING RULES. None

3.1.4.6. POWER SUPPLY REQUIREMENTS. +5 volt supply. Resistors R1, R6, and R8 draw current from the +5 volt supply.

$$\overline{I_{R1}} = \frac{V_1 - V_{CE1} - I_{e1}R7}{R1} = 606 \text{ microamperes}$$

$$\overline{I_{R6}} = \frac{I_{e2}R8 + V_{BE2}}{R6} = 142 \text{ microamperes}$$

$$\overline{I_{R8}} = I_{e2} \qquad\qquad = 2300 \text{ microamperes}$$

$$\text{Total} = 3048 \text{ milliamperes}$$

3.1.5. INVERTING AND AMPLIFYING CIRCUITS

Specifications

 a. Gate-In Pulse—provides low-impedance output at ground level when either of two inputs is at +5 volts; provides high-impedance output when both inputs are at ground. Drive load of 70 microamperes.

 b. Gate-Out Pulse—supplies 150 microamperes at +5 volt level with an input at ground.

 c. Counter Step Pulse—supplies one milliampere at -5 volt level with an input at ground.

3.1.5.1. DESCRIPTION. The gate-in circuit (Figure 14) consists of a positive AND gate and an inverter. Both of these circuits are discussed elsewhere in this report. The remainder of this group of circuits consists of inverting amplifiers.

3.1.5.2. DESIGN PROCEDURE. The base resistor values were chosen to provide sufficient base drive, and the coupling capacitors were chosen to provide sufficient overdrive to meet speed requirements. The collector resistors were made small enough to provide a reasonable turn-off time.

3.1.5.3. EQUATIONS OF OPERATION. Equations will be written for the gate-out pulse. All parameters are included in the table under the next heading.

$$I_{C1} = \frac{V_1 - V_{CE1}}{R3} + I_{LOAD} \tag{9}$$

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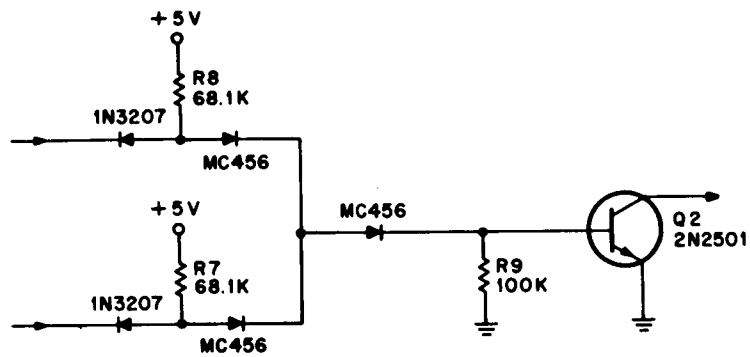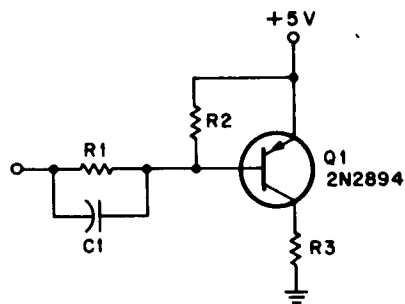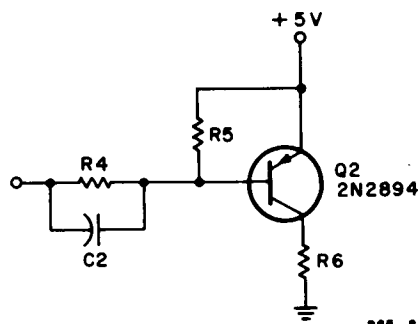
Figure 14. Inverting and Amplifying Circuits

$$I_{B1} = \frac{V_1 - V_{BE1} - V_{IN}}{R1} - \frac{V_{BE1}}{R2} \qquad (10)$$

3.1.5.4. CALCULATIONS. Currents I_{C1} and I_{B1} can be found with the following conditions at $-20^{\circ}C$ from equations (9) and (10).

$V_1 = \underline{V_1} = 4.8$ volts $\qquad V_{IN} = \overline{V_{IN}} = 0.3$ volt $\qquad I_{LOAD} = 150$ microamperes

$R1 = \overline{R1} = 35K \qquad R2 = \underline{R2} = 17.3K \qquad R3 = \underline{R3} = 21.4K$

$V_{CE1} = 0.3$ volt $\qquad V_{BE1} = \overline{V_{BE1}} = 1.04$ volts

$I_{C1} = 360$ microamperes $\qquad \underline{I_{B1}} = 39$ microamperes

| Pulse | NOMINAL VALUE | | | | at $-20^{\circ}C$ | | | |
	R1	R2	R3	C_1	$I_B \quad I_C$ (in micro-amperes)	I_{load}	Required h_{FE}
Gate Out	26.7K	20.0K	22.1K	10 pf	39 360	150 μA	9.2
Counter Step Pulse	10.0K	10.0K	5.62K	18 pf	224 1800	1 MA	8.1

3.1.5.5. DEVIATIONS FROM DERATING RULES. None

3.1.5.6. POWER SUPPLY REQUIREMENTS. +5 volt supply.

Pulse	Standby	100 KC	Duty Cycle
Gate-out	0	41.8 μA	0.1
Counter step	0	0.3 MA	0.15
Gate-in	142 μA	142 μA	—
Total	142 μA	0.623 MA	

3.1.6. DELAY FLOP—TYPE F AND TYPE S

Specifications

a. Dissipate zero standby power

b. Provide a pulse width with a tolerance of ±5 percent initially and ±10 percent E.O.L. over the specified temperature range.

c. Trigger on a negative-going edge starting at +5 volts and going more negative than +1.8 volts.

d. Input trigger current:

Type S - 0.2 milliampere
Type F - 0.6 milliampere

e. Output drive capability:

Type S - 3 milliamperes
Type F - 12 milliamperes

3.1.6.1. DESCRIPTION. Transistors Q1 and Q2 (Figure 15) are connected as a conventional monostable multivibrator or delay flop with a few modifications. In a strictly conventional delay flop, Q2 is normally biased on and is turned off when the delay flop is triggered. After a capacitor is charged, Q2 turns on again and ends the period of the delay flop. Since no standby power is a requirement in this application, Q2 is not biased on. However, the period of this delay flop is determined the same way as in a conventional delay flop.

Figure 15. Delay Flop, Types F and S

Transistors Q1, Q2, and Q3 are all off when a negative input is applied to C_3; this causes Q3 to conduct. The collector of Q3 is connected to the bases of Q1 and Q2, but the components are adjusted in such a manner as to ensure that Q1 begins to conduct first. Current flows from the collector of Q3 through R4, D1, and D2 into the base of Q1 and through R5, C_2, and the collector of Q1. Base current for Q3 is now supplied by Q1 through R6; this

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current causes Q1 and Q3 to latch. The input must be long enough to ensure this latchup. The base of Q2 is quiescent at ground potential. When Q1 turns on, the collector of Q1 drops V_1 volts in potential. This drop is coupled to the base of Q2 through C_2 and causes the potential at the base of Q2 to be minus V_1 volts. The potential charges towards $+V_1$ volts since C_2 is being charged to $+V_1$ through the collector-emitter junction of Q1. When the potential at the base of Q2 reaches $V_{BE_{ON}}$, Q2 conducts and diverts the base current of Q1 through R4 and D3. Transistor Q1 now turns off and causes Q3 to turn off. Since Q3 is off, Q2 now turns off, and C_2 recharges through R8, R5, and R2. Since Q2 turned on momentarily, the collector of Q2 can be used to trigger another delay flop. A negative output can be taken from the collector of Q1 while the collector of Q2 can only be used to trigger other delay flops.

3.1.6.2. DESIGN PROCEDURE. (Type F will be discussed, and Type S is identical except for values). Resistor R4 was selected to provide sufficient base drive to Q1 to enable Q1 to drive the required load of 12 milliamperes. Resistor R5 was selected to drive Q2 so that Q2 can drive a delay flop input as well as absorb the current from R4. Capacitor C_2 can now be selected to give the required pulse width.

$$T = C_2 R5 \ln \frac{2V_1 - V_{CE1} - V_{BE1} + I_{B12}(R5-R8)}{V_1 + I_{B12}R5 - V_{BE2}} \tag{11}$$

$$T = 0.69 C_2 R5 \tag{12}$$

The drops across Q1, D1, D2, D3 are neglected in equation (11), and all semiconductor drops and leakage current are neglected in equation (12).

Resistor R3 is used to charge the input capacitor C_3 of the next stage. Resistor R6 supplies base current to Q3 from Q1 to cause Q1 and Q3 to latch.

Resistor R8 recharges C_3 after a delay flop on period.

Resistors R7, R2, and R1 supply d-c returns to ground for base leakage current for Q1, Q2, and Q3, respectively. Diodes D1 and D2 are level-shift diodes.

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3.1.6.3. EQUATIONS OF OPERATION. Base current of Q1:

$$\frac{V_1 - V_{CE3} - V_{D1} - V_{D2} - V_{BE1}}{R4} - \frac{V_{BE1}}{R7} - I_{CO2}$$

Base current of Q2:

$$\frac{V_1 - V_{CE3} - V_{BE2}}{R5}$$

Base current of Q3:

$$\frac{V_1 - V_{BE3} - V_{CE1}}{R6} - \frac{V_B E_3}{R1} - \frac{V_1}{R3} \qquad \text{current recharging } C_3 \text{ subtracts from base current.}$$

Collector current of Q1:

$$\frac{V_1 - V_{CE1}}{R8} + \frac{V_1 - V_{BE3} - V_{CE1}}{R6} + \frac{2V_1 - V_{CE3} - V_{CE1}}{R5} + I_{LOAD}$$

Collector current of Q2:

$$\frac{V_1 - V_{CE2}}{R3} + \frac{V_1 - V_{CE3} - V_{D3} - V_{CE2}}{R4} + I_{trigger}$$

Collector current of Q3:

$$\frac{V_1 - V_{CE3}}{R2} + \frac{V_1 - V_{CE3} - V_{D1} - V_{D2} - V_{BE1}}{R4} + \frac{2V_1 - V_{CE3} - V_{CE1}}{R5}$$

3.1.6.4. CALCULATIONS.

R1 22.1K	R5 30K nominal	C_1 10 picofarads
R2 22.1K	R6 8.45K	C_2 variable
R3 22.1K	R7 26.7K	C_3 33 picofarads
R4 5.23K	R8 2.37K	

$-20^\circ C$ (4S)

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$$I_{B1} = \frac{4.8 - 0.3 - 0.95 - 1.0}{(5.23)(1.03)(10^3)} - \frac{1}{26.7(0.9)(10^3)}$$

$$= 0.297 - 0.04$$

$$= 0.257 \text{ milliampere}$$

$$I_{C1} = \frac{4.8 - 0.3}{2.37(0.97)(10^3)} + \frac{4.8 - 0.84 - 0.3}{8.45(0.97)(10^3)} + \frac{9.6 - 0.3 - 0.3 + 0.5(10^{-3})}{30(0.97)(10^3)}$$

$$= 1.95 + 0.447 + 0.31 + 0.5$$

$$= 3.2 \text{ milliamperes}$$

-20°C (4S)

$$I_{B2} = \frac{4.8 - 0.3 - 1.0}{30(1.03)(10^3)}$$

$$= 0.113 \text{ milliampere}$$

Current required to trigger blocking oscillator:

$$I_{C2} = \frac{4.8 - 0.3}{22.1(0.97)(10^3)} + \frac{4.8 - 0.3 - 0.79 - 0.3}{5.23(0.97)(10^3)} + 0.4 \text{ milliampere}$$

$$= 0.21 + 0.67 + 0.4$$

$$= 1.28 \text{ milliamperes}$$

-20°C (4S)

$$I_{B3} = \frac{4.8 - 1.28 - 0.3}{8.45(1.03)(10^3)} - \frac{1.28}{22.1(0.97)(10^3)} - \frac{4.8}{22.1(0.97)(10^3)}$$

$$= 0.372 - 0.06 - 0.224$$

$$= 0.092 \text{ milliampere}$$

$$I_{C3} = \frac{4.8 - 0.3}{22.1(0.97)(10^3)} + \frac{4.8 - 0.3 - 0.87 - 0.87 - 1}{5.23(0.97)(10^3)} + \frac{9.6 - 0.3 - 0.3}{30(0.97)(10^3)}$$

$$= 0.21 + 0.347 + 0.31$$

$$= 0.867$$

-20°C (4F)

R1 39.2K	R5 7.5K nominal	C_1 10 picofarads
R2 22.1K	R6 8.45K	C_2 variable
R3 22.1K	R7 26.7K	C_3 44 picofarads
R4 1.65K	R8 10K	

$$\underline{I_{B1}} = \frac{4.8 - 0.3 - 0.95 - 0.95 - 1.1}{1.65(1.03)(10^3)} - \frac{1.1}{26.7(0.97)(10^3)}$$

$$= 0.88 - 0.04$$

$$= 0.84 \text{ milliampere}$$

$$I_{C1} = \frac{4.8 - 0.3}{10(10^3)(0.97)} + \frac{4.8 - 0.84 - 0.3}{8.45(0.97)(10^3)} + \frac{9.6 - 0.3 - 0.3}{7.5(0.97)(10^3)} + 7.6$$

$$= 0.465 \pm 0.446 + 1.24 + 7.6$$

$$= 9.75 \text{ milliamperes}$$

-20°C (4F)

$$\underline{I_{B2}} = \frac{4.8 - 0.3 - 1.03}{7.5(1.03)(10^3)}$$

$$= 0.45 \text{ milliampere}$$

$$I_{C2} = \frac{4.8 - 0.3}{49.9(0.97)(10^3)} + \frac{4.8 - 0.3 - 0.84 - 0.3}{1.15(0.97)(10^3)} + 2\text{-milliampere trigger}$$

$$= 0.092 + 2.1 + 2 + 1.7 \text{ (milliamperes for discharge transistor)}$$

$$= 5.89 \text{ milliamperes}$$

-20°C (4F)

$$I_{B3} = \frac{4.8 - 1.28 - 0.3}{8.45(1.03)(10^3)} - \frac{1.03}{39.2(0.97)(10^3)} - \frac{4.8}{49.9(0.97)(10^3)}$$

$$= 0.37 - 0.027 - 0.09$$

$$= 0.25$$

$$I_{C3} = \frac{4.8 - 0.3}{22.1(10^3)(0.97)} + \frac{4.8 - 0.3 - 0.84 - 0.84 - 0.75}{1.65(0.97)(10^3)} + \frac{9.6 - 0.3 - 0.3}{7.5(0.97)(10^3)}$$

$$= 0.1 + 1.25 + 1.24$$

$$= 2.7$$

3.1.7. READ/WRITE TRIGGER GATE

Specifications

a. Output capability—output 1, 2.1 milliamperes; output 2, 4.5 milliamperes.

b. Input requirements—A and B, 0.5 milliampere; C, D, and E, 0.45 milliampere.

c. Power dissipation—10 milliwatts peak, zero standby.

3.1.7.1. DESCRIPTION. Output 1 (Figure 16) varies from +5 volts to approximately ground with the following input conditions:

Point E—Ground

Point B—+5 volts

Point A—+5 volts

Output 2 varies from +5 volts to approximately ground with the following input conditions:

Point E—Ground		Point E—Ground
Point B—+5 volts	or	Point D—+5 volts
Point A—+5 volts		Point C—+5 volts

The outputs are used to drive the input capacitor of a delay-flop; R3 and R4 recharge the input capacitor. The input to Q4 and Q5 is a positive AND gate.

3.1.7.2. DESIGN PROCEDURE. One objective of the circuit was to dissipate zero standby power. Inputs A, B, C, and D are levels, and E is a pulse.
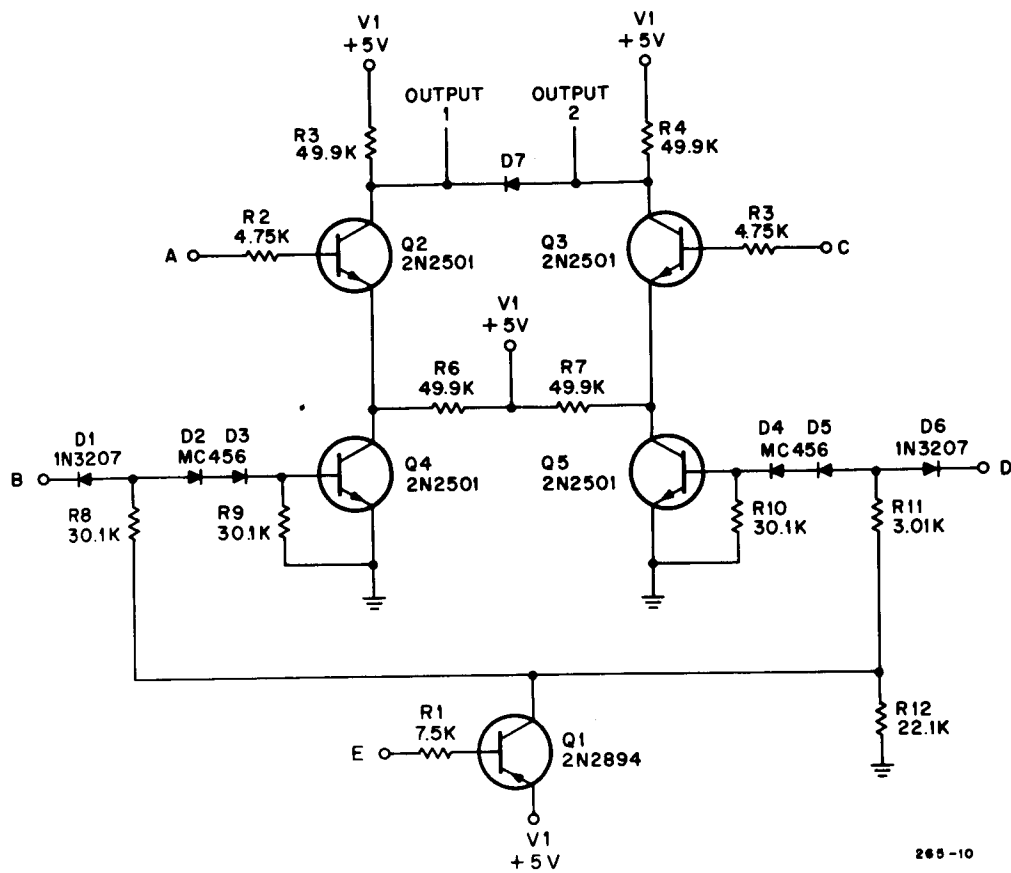
Figure 16. Read-Write Trigger Gate

Therefore, current will flow only when input E is present, thereby allowing zero standby power. Inputs B and D are complementary. Inputs A and C are mutually exclusive inputs. Diode D7 allows output 2 to go low when Q2 and Q4 conduct or when Q3 and Q5 conduct. Output 1 will go low only when Q2 and Q4 conduct.

3.1.7.3. EQUATIONS OF OPERATION.

$$I_{B1} = \frac{V_1 - \overline{V_E} - \overline{V_{BE1}}}{\overline{R1}}$$

$$I_{B2} = \frac{V_A - \overline{V_{BE2}} - \overline{V_{CE4}}}{\overline{R2}}$$

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3.1.7.4. CALCULATIONS.

-20°C

$$I_{B1} = \frac{4.8 - 0.3 - (0.8+0.11)(1.2)}{(7.5)(10^3)(1.03)} = 0.44 \text{ milliampere} = I_{B3}$$

$$I_{B2} = \frac{3.75 - (0.8+0.11)(1.2)}{(4.75)(10^3)(1.03)} = 0.55 \text{ milliampere}$$

$$I_{B4} = \frac{4.8 - 0.3 - (0.67+0.11)(1.2) \times 2 - (0.8+0.11)(1.2)}{(3.01)(10^3)(1.03)} - \frac{(0.8+0.11)(1.2)}{(30.1)(10^3)(0.97)}$$

$$= 0.47 \text{ milliampere} = I_{B5}$$

$$I_{B4} = \frac{V_1 - \overline{V_{CE1}} - \overline{V_{D2}} - \overline{V_{D3}} - \overline{V_{BE4}}}{\overline{R8}} - \frac{V_{BE4}}{\overline{R9}} - I_e D1$$

$$I_{B3} = I_{B2} \qquad\qquad I_{B5} = I_{B4}$$

$$I_{C1} = \frac{V_1 - \overline{V_{CE1}} - \underline{V_{D2}} - \underline{V_{D3}} - \underline{V_{BE4}}}{\underline{R8}} + \frac{V_1 - \overline{V_{CE1}} - \underline{V_{DG}} - \underline{V_D}}{R11} - \frac{V_1 - \overline{V_{CE1}}}{R12}$$

$$I_{C2} = \frac{V_1 - \overline{V_{CE2}} - \underline{V_{CE4}}}{\underline{R3}} + \text{Load 1} + \text{Load 2}$$

$$I_{C4} = I_{C2} + \frac{V_1 - \overline{V_{CE4}}}{\underline{R6}}$$

$$I_{C3} = \frac{V_1 - \overline{V_{CE3}} - \underline{V_{CE5}}}{\underline{R4}} + \text{Load 2}$$

$$I_{C5} = I_{C3} + \frac{V_1 - \overline{V_{CE5}}}{\underline{R7}}$$

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$$I_{C1} = \frac{4.8 - 0.3 - (0.67+0.11)(0.8) \times 2 - (0.8+0.11)(0.8)}{(3.01)(10^3)(0.97)}$$

$$+ \frac{4.8 - 0.3 - (0.57+0.11)(0.8)}{(3.01)(10^3)(0.97)} + \frac{4.8 - 0.3}{(22.1)(10^3)(0.97)} = 2.8 \text{ milliamperes}$$

$$I_{C2} = \frac{4.8 - 0.3 - 0.23}{(49.9)(10^3)(0.97)} + 1 \text{ milliampere} + 3.4 \text{ milliamperes}$$

$$= 0.088 + 4.4$$

$$= 4.5 \text{ milliamperes}$$

$$I_{C4} = 4.6 \text{ milliamperes}$$

$$I_{C3} = 3.5 \text{ milliamperes}$$

$$I_{C5} = 3.5 \text{ milliamperes}$$

Minimum h_{FE}

$$Q1 \quad h_{FE} = \frac{2.8}{0.44} = 6.4$$

$$Q2 \quad h_{FE} = \frac{4.5}{0.55} = 8.2$$

$$Q3 \quad h_{FE} = \frac{3.5}{0.44} = 8.0$$

$$Q4 \quad h_{FE} = \frac{4.6}{0.47} = 10$$

$$Q5 \quad h_{FE} = \frac{3.6}{0.47} = 7.7$$

3.1.8. SENSE AMPLIFIER AND BIT-DRIVER GATE

Specifications

a. Output capability—output C, 40 milliamperes; output D, 21 milli-
amperes.

b. Input requirements—A, 4 milliamperes; B, 1.5 milliamperes.

3.1.8.1. DESCRIPTION. Input A (Figure 17) is a negative-going pulse, +5 volts to ground, from a delay flop. If Q2 is off when input A occurs, Q1 will conduct. The base current for Q1 flows through D2 and R2 to input A. If input B were at ground (which would cause Q2 to conduct) input A would not cause Q1 to conduct because point X would not be sufficiently negative to allow D2 to conduct. Input B at ground would also cause Q3 to conduct; its base current is supplied through R4 and Q2.
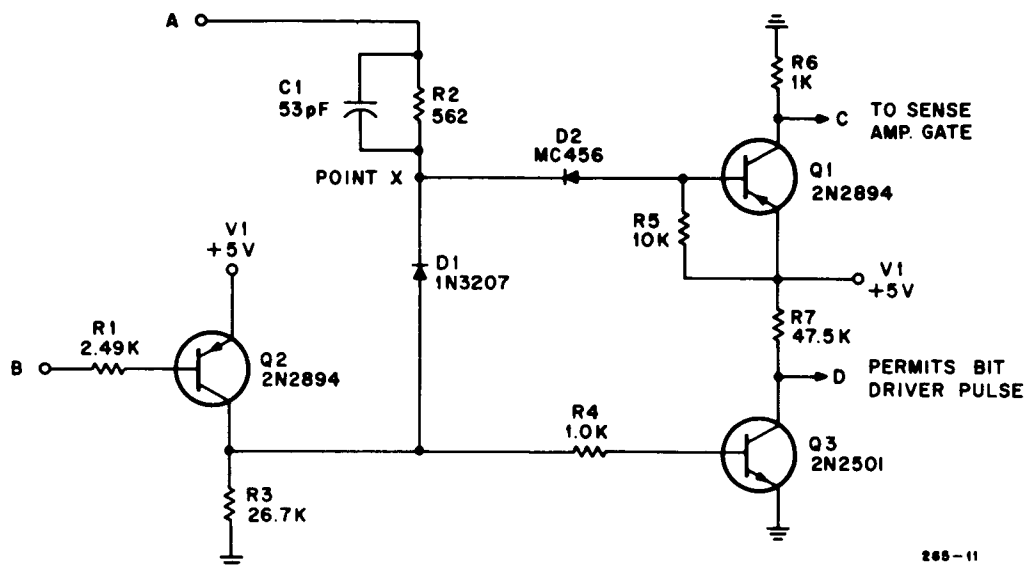

Figure 17. Sense Amplifier and Bit Driver Gate

The base of Q2 is returned to +5 volts by means of a 10K resistor located at the driving end. Diode D1 prevents d-c flow from input A when it is at +5 volts into the base of Q3. Diode D2 is a level-shift diode.

3.1.8.2. EQUATIONS.

At $-20^{\circ}C$

$$I_{B1} = \frac{V_1 - V_A - \overline{V_{D2}} - \overline{V_{BE1}}}{\overline{R2}} - \frac{\overline{V_{BE1}}}{\overline{R5}}$$

$$I_{B2} = \frac{V_1 - \overline{V_B} - \overline{V_{BE2}}}{\overline{R1}}$$

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$$I_{B3} = \frac{V_1 - \overline{V_{CE2}} - \overline{V_{BE3}}}{\overline{R4}}$$

$$I_{C1} = \frac{V_1 - \overline{V_{CE1}}}{\underline{R6}} + I_{load_{Q1}}$$

$$I_{C2} = \frac{V_1 - V_{CE2} - \underline{V_{D1}} - \underline{V_A}}{\underline{R2}} + \frac{V_1 - \overline{V_{CE2}} - \underline{V_{BE3}}}{\underline{R4}}$$

$$I_{C3} = \frac{V_1 - \overline{V_{CE3}}}{\underline{R7}} + I_{load_{Q3}}$$

$$I_{B1} = \frac{4.8 - 0.3 - (0.75+0.11)(1.2) - (1+0.11)(1.2)}{561(1.03)} - \frac{(0.8+0.11)(1.2)}{104(0.97)}$$

$$= 3.82 - 0.112 = 3.7 \text{ milliamperes}$$

$$I_{B2} = \frac{4.8 - 0.3 - (0.8+0.11)(1.2)}{2.49(10^3)(1.03)} = 1.33 \text{ milliamperes}$$

$$I_{B3} = \frac{4.8 - 0.3 - (1+0.11)(1.2)}{10^3(1.03)} = 3.1 \text{ milliamperes}$$

$$I_{C1} = \frac{4.8 - 0.3}{10^3(0.97)} + 40 \text{ milliamperes} = 44.6$$

$$I_{C2} = \frac{4.8 - 0.3 - (0.7+0.11)(0.8)}{562(0.97)} + \frac{4.8 - 0.3 - (1+0.11)(0.8)}{10^3(0.97)}$$

$$= 7.2 + 3.7$$

$$= 10.9$$

$$I_{C3} = \frac{4.8 - 0.3}{47.5(10^3)(0.97)} + 21 \text{ milliamperes}$$

$$= 21.1 \text{ milliamperes}$$

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Minimum h_{FE} required

$$Q1 \quad h_{FE} = \frac{I_{C1}}{I_{B1}} = \frac{44.6}{3.7} = 12$$

$$Q2 \quad h_{FE} = \frac{I_{C2}}{I_{B2}} = \frac{9.9}{1.33} = 7.5$$

$$Q3 \quad h_{FE} = \frac{I_{C3}}{I_{B3}} = \frac{21}{3.1} = 6.8$$

3.1.9. HIGH-POWER DRIVERS

Specifications

A. A-Switch/Driver

    a. Output capability—200 milliamperes at +24 volts; t_r 12 nanoseconds; t_f 25 nanoseconds.

    b. Input requirements—7.5 milliamperes at ground.

B. Bit-Driver Pulse

    a. Output capability—200 milliamperes at +12 volts; t_r and t_f 15 nanoseconds.

    b. Input requirements—7.5 milliamperes at ground.

C. A- and B-Counter Drive Pulse

    a. Output capability—A-counter/driver—5 milliamperes + 12.7 milliamperes.

          —B-counter/driver—25 milliamperes.

    b. Input requirements—7 milliamperes at ground.

D. P-Counter Drive Pulse and P-Switch Pulse

    a. Output capability—P-counter/driver—5 milliamperes.

          —P-switch pulse—50 milliamperes.

    b. Input requirements—2.4 milliamperes.

E. Regulator Driver

    a. Output capability—100 milliamperes at +5 volts.

    b. Input requirements—12.7 milliamperes at +5 volts.

3.1.9.1. DESCRIPTION. Complementary stages are used to reduce the standby power to zero. There are, at present, no silicon PNP transistors available that have the gain-bandwidth product required in the output stage of the drivers shown in Figures 18, 19, and 22. Since a positive output pulse is required, an NPN transistor and a transformer must be used.
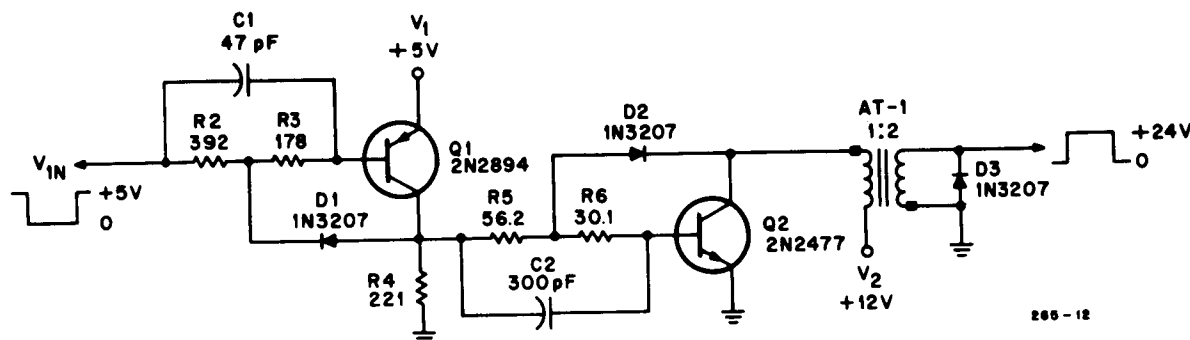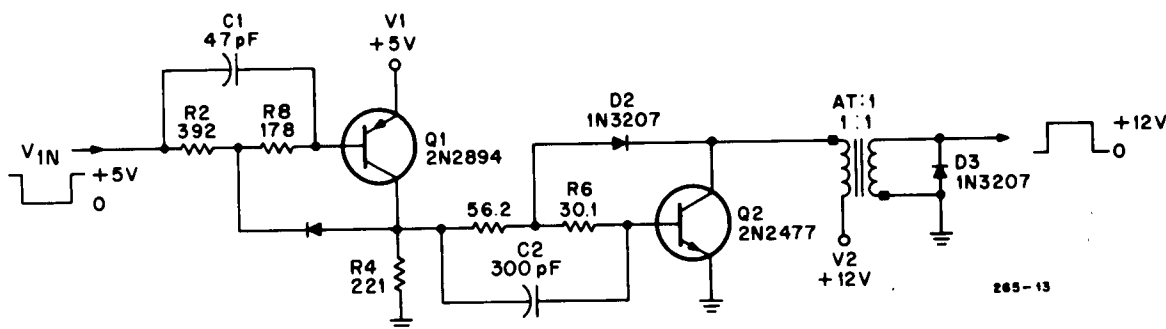

Figure 18. A-Switch Driver

Figure 19. Bit-Driver Pulse

In circuit C (Figure 20), the input varies from +5 volts to ground and cannot drive the output stage directly because the emitter of the output stage is returned to +12 volts. An alternate to the transformer coupling is shown in Figure 23. It is felt that the transformer approach was the more economical of the two.

Circuit D (Figure 21) is similar to C (Figure 20) except that an additional stage is needed to achieve the required gain.

Back-clamping is used in circuits A, B, and D (Figures 18, 19, and 22) to prevent deep saturation which results in long storage times. Speed-up capacitors are used in most cases to provide overdrive during turn-on and clean-up current during turn-off. Each transformer is shunted with a diode
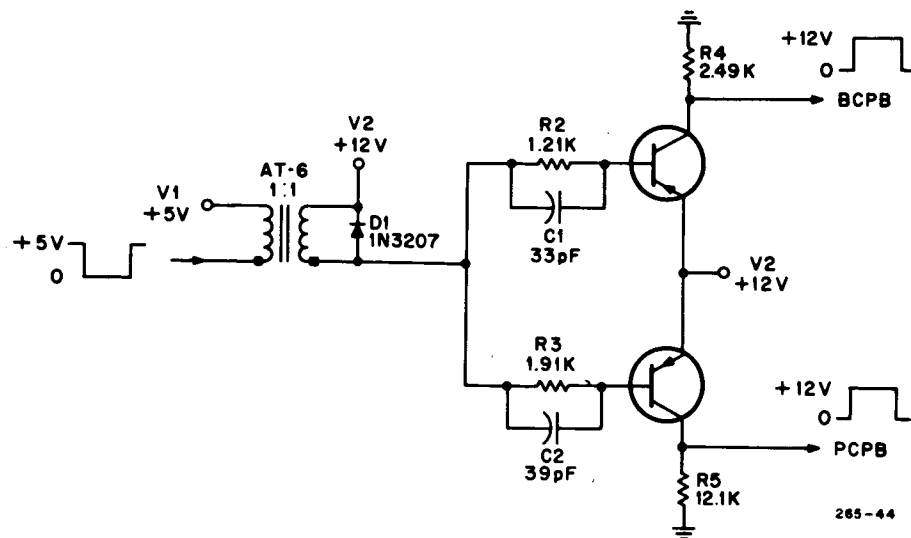
44

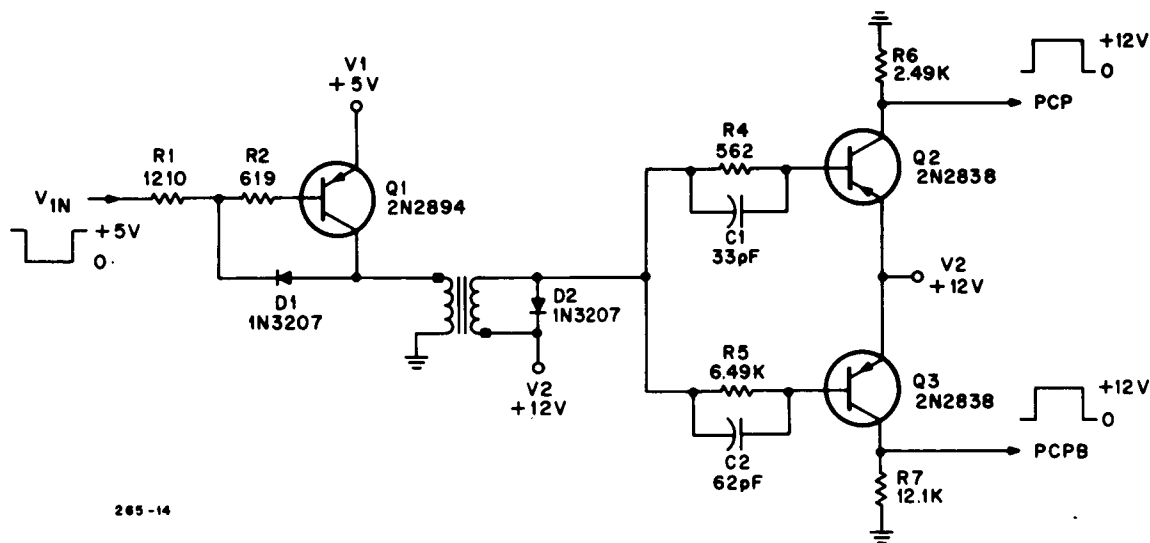Figure 20. A- and B-Counter Drive Pulse

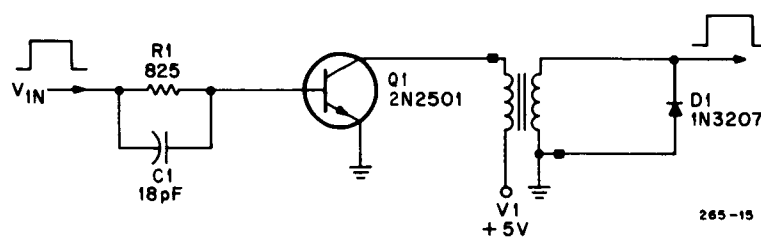Figure 21. P-Counter Drive Pulse and P-Switch Pulse
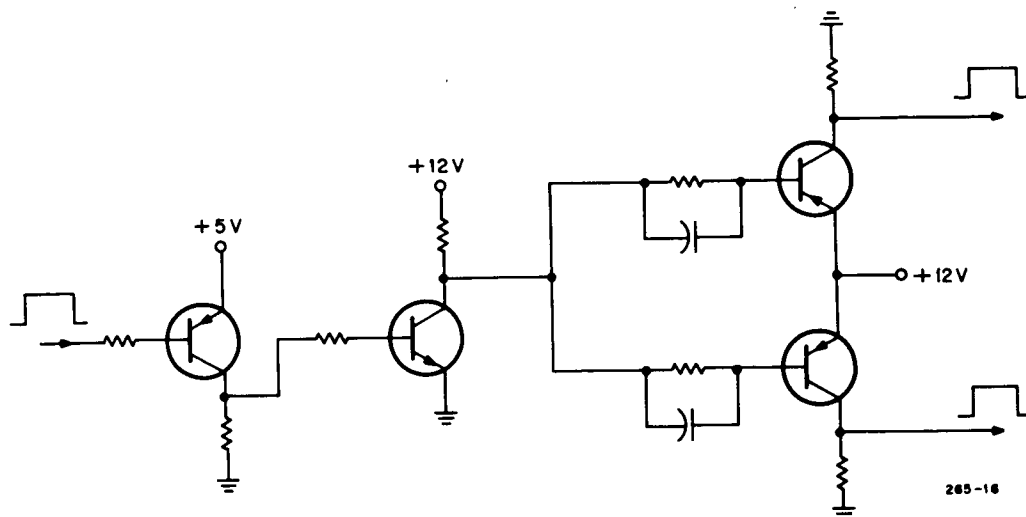

Figure 22. Regulator Driver

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Figure 23. Alternate Coupling Arrangement for Drivers

to protect the transistors during transformer recovery. There is no problem with recovery time because the maximum duty cycle used is one out of 300, and the maximum allowable is one out of 30.

3.1.9.2. EQUATIONS AND CALCULATIONS. The equations are written for the case in which all back clamping diodes are removed. If the base current is sufficient with the diodes removed, it is more than sufficient with the diodes in because V_{CE} will increase and less base current will be required for a given collector current.

$-20^{\circ}C$

Circuit A

$$\underline{I_{B1}} = \frac{V_1 - \overline{V_{IN}} - \overline{V_{BE}}}{R2 + R3} = \frac{4.8 - 0.3 - (1.2+1.1)(1.2)}{(392+178)(1.03)} = 4.97 \text{ milliamperes}$$

$$\underline{I_{C1}} = \frac{V_1 - \overline{V_{CE1}}}{\underline{R4}} + \frac{V_1 - \overline{V_{CE1}} - V_{BE2}}{\underline{R5} + \underline{R6}} + \frac{4.8 - 0.7}{221(0.97)} + \frac{4.8 - 0.7 - (1+0.11)(8)}{(56.2+30.1)(0.97)}$$

$$= 57.6 \text{ milliamperes}$$

$$\text{Minimum } h_{FE} = \frac{57.6}{4.97} = 11.5$$

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$$I_{B2} = \frac{V_1 - \overline{V_{CE1}} - \overline{V_{BE2}}}{\overline{R5} + \overline{R6}} = \frac{4.8 - 0.7 - (1+0.11)(1.2)}{56.2+30.1)(1.03)} = 31.5$$

$$I_{C2} = I_{load} + I_{magnetizing}$$

$$I_{mag} = \frac{V(\overline{P})}{\underline{L}} = \frac{(12)(0.96) \times 0.250(10^{-6})}{60(10^{-6})} = 48 \text{ milliamperes}$$

$$I_{load} \text{ reflected in primary} = 320 \text{ milliamperes}$$

$$I_{C2} = 368 \text{ milliamperes}$$

$$\text{Minimum } h_{FE} = \frac{368}{31.5} = 11.7$$

Circuit B. Same as circuit A except that the transformer turns ratio is 1:1.

Circuit C

$$I_{B1} = \frac{V_2 - \overline{V_{BE1}} - \overline{V_{IN}}}{\overline{R3}} = \frac{4.8 - (1+0.11)(1.2) - 0.3}{(1.91)(10^3)(1.03)} = 1.63$$

$$I_{C1} = \frac{V_2 - \overline{V_{CE1}}}{\overline{R5}} + I_{load} = \frac{11.52 - 0.3}{12.1(10^3)(0.97)} + 17.7 = 18.3 \text{ milliamperes}$$

$$\text{Minimum } h_{FE} = \frac{18.3}{1.63} = 11.2$$

$$I_{B2} = \frac{V_2 - \overline{V_{BE1}} - \overline{V_{IN}}}{\overline{R2}} = \frac{4.8 - (1+0.11)(1.2) - 0.3}{(1.21)(10^3)(1.03)} = 2.6 \text{ milliamperes}$$

$$I_{C2} = \frac{V_2 - \overline{V_{CE1}}}{\underline{R4}} + I_{load} = \frac{11.52 - 0.3}{2.49(10^3)(0.97)} + 25 = 29.6 \text{ milliamperes}$$

$$\text{Minimum } h_{FE} = \frac{29.6}{2.6} = 11.4$$

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Circuit D

$$I_{B1} = \frac{V_1 - \overline{V_{BE1}} - \overline{V_{IN}}}{\overline{R1} + \overline{R2}} = \frac{4.8 - (1+0.11)(1.2) - 0.3}{(1210+619)(1.03)} = 1.7$$

$$I_{C1} = \frac{V_1 - V_{BE2}}{\underline{R4}} + \frac{V_1 - V_{BE3}}{\underline{R5}} + \frac{(V_1)(P.\overline{W}.)}{\underline{L_P}}$$

$$= \frac{4.8 - (1+0.11)(0.8)}{562(0.97)} \quad \frac{4.8 - (1+0.11)(0.8)}{6.49(10^3)(0.97)} \quad \frac{(4.8)(1.9)(10^{-6})}{680(10^{-6})}$$

$$= 7.2 + 0.62 + 0.134 = 7.83 \text{ milliamperes}$$

$$\text{Minimum } h_{FE} = \frac{7.82}{1.7} = 4.5$$

$$I_{B2} = \frac{V_1 - \overline{V_{BE2}}}{\overline{R4}} = \frac{4.8 - (1+0.11)(1.2)}{562(1.03)} = 6 \text{ milliamperes}$$

$$I_{C2} = \frac{\overline{V_2} - \overline{V_{CE2}}}{\underline{R6}} + I_{load} = \frac{12.48 - 0.3}{2.49(10^3)(0.97)} + 50 \text{ milliamperes} = 55 \text{ milli-amperes}$$

$$\text{Minimum } h_{FE} = \frac{55}{6} = 9.2$$

$$I_{B3} = \frac{V_1 - V_{BE3}}{\overline{R5}} = \frac{4.8(1+0.11)(1.2)}{6.49(10^3)(1.03)} = 0.52 \text{ milliamperes}$$

$$I_{C3} = \frac{\overline{V_2} - \overline{V_{CE2}}}{\underline{R7}} + I_{load} = \frac{12.48 - 0.3}{12.1(10^3)(0.97)} + 5 \text{ milliamperes} = 6 \text{ milli-amperes}$$

$$\text{Minimum } h_{FE} = \frac{6}{0.52} = 11.5$$

Circuit E

$$I_{B1} = \frac{V_{IN} - \overline{V_{BE}}}{\overline{R1}} = \frac{(11.52-0.3) - (1+0.11)(1.2)}{825(1.03)} = 12 \text{ milliamperes}$$

$$I_{C2} = I_{load} + I_m = I_{load} + \frac{V_1 \overline{(P.W.)}}{\underline{L_p}}$$

$$= 100 \text{ milliamperes} + \frac{(5.2)(0.3 \times 10^{-6})}{680(10^{-6})}$$

$$= 102.3 \text{ milliamperes}$$

$$\text{Minimum } h_{FE} = \frac{102.3}{12} = 8.5$$

Transformer data

$$L_{primary\ required} = \frac{(Voltage)(Pulse\ Width)}{(Allowable\ magnetizing\ current)}$$

Inductance is derated 20 percent due to initial permeability variation, 25 percent due to temperature.

Therefore,

$$L = \frac{VT}{1} \times 1.2 \times 1.25 = 1.5 \frac{VT}{I}$$

        core material T-1:   Indiana General
        core size: 101

Circuit A

    $V = 12$ volts $T = 0.150$ microsecond $I_m = 30$ milliamperes

    $L = 60 \times 1.5 = 90$ microhenries $N_p = 15$ $N_s = 30$

Circuit B. Same as circuit A: $N_p = 15$, $N_s = 30$

Circuit C

    $V = 5$ volts $T = 0.55$ microsecond $I_m = 4$ milliamperes

    $L = 685 \times 1.5 = 1028$ microhenries $N_p = 50$ $N_s = 50$

Circuit D

V = 5 volts   T = 1.9 microsecond I_m = 14 milliamperes

L = 680 × 1.5 = 1020 microhenries N_p = 50 N_s = 50

Circuit E

V = 5 volts   T = 0.55 microsecond I_m = 4 milliamperes

L = 685 × 1.5 = 1028 microhenries N_p = 50 N_s = 50

3.1.9.3. EFFECT OF BACK-CLAMPING. The addition of a back-clamping diode re-
sults in higher V_{CE}, lower required base drive, and less storage time. In
Figure 24, V_{CE} is given by the following equation:

$$V_{CE} = \frac{V_1 R1R2 + V_2 R2R_L + (V_{BE} - V_{D1})(R1R_L)(1 + h_{FE}) - V_D R2P_L}{R1R2 + R_L R + (1 + h_{FE})(R1R2)} \tag{13}$$

for V_1 = 12, V_2 = 5 volts, V_{BE} = 1 volt, V_{D1} = 0.67 volt

$$V_{CE} = \frac{28 + 0.67\, h_{FE}}{5 + 2\, h_{FE}} \tag{14}$$

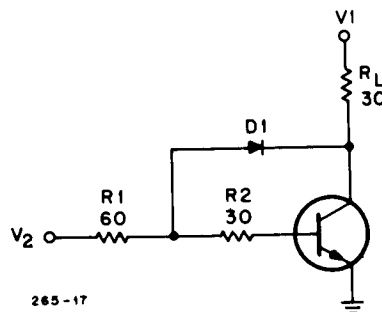where h_{FE} is $\dfrac{I_C}{I_B}$ or circuit beta.

Figure 24. Connection of
Back-Clamping Diode

This calculation is plotted in Figure 25 along with transistor beta
versus V_{CE}. The intersection of these two plots gives the operating point
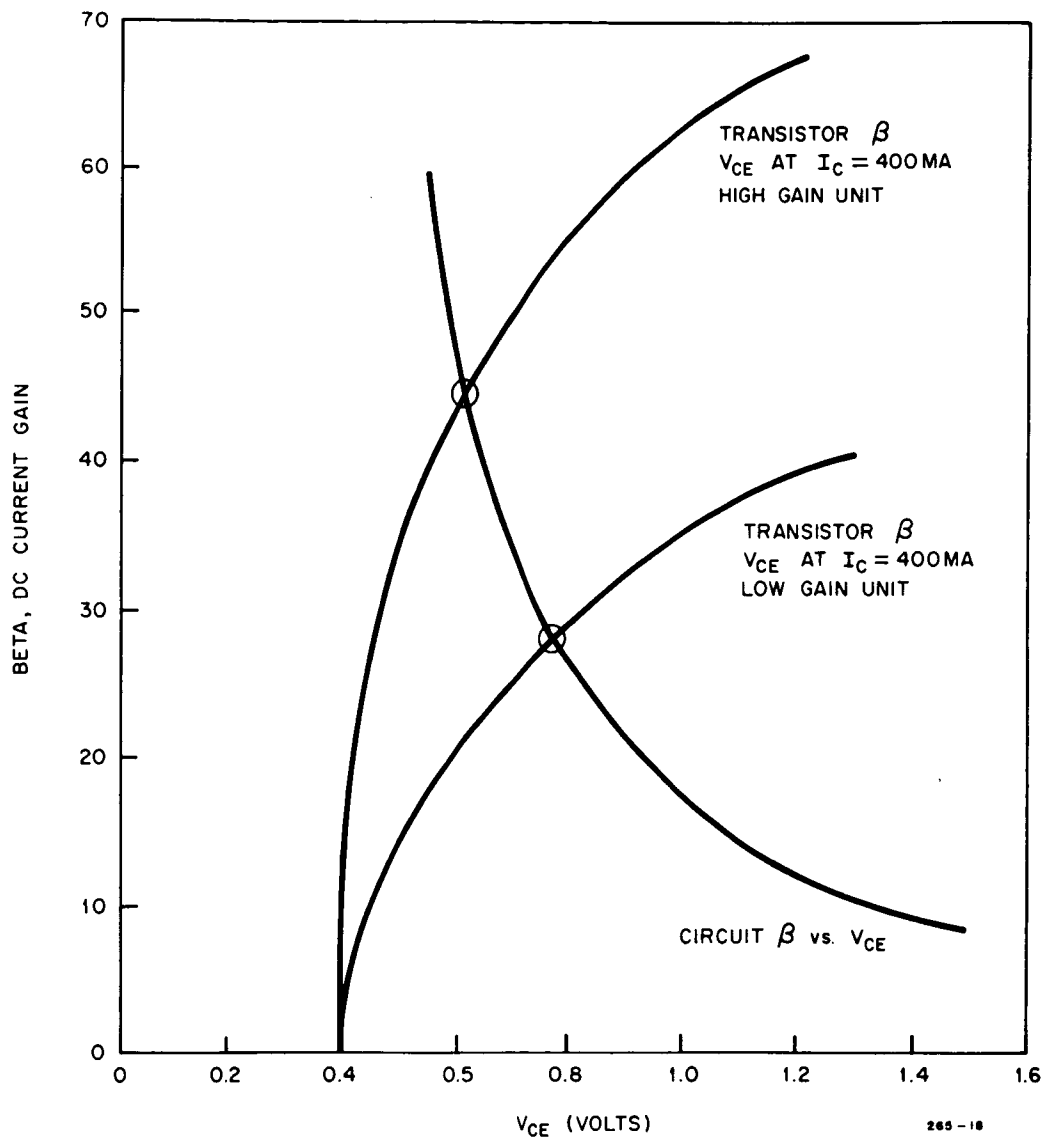of the transistor.

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Figure 25. Transistor and Circuit Beta Versus V_{CE}

3.1.10. SIGNAL INVERTERS

Specifications

a. Counter step pulse inverter

b. Clock amplifier and data output driver

c. Read and write signal inverter and memory clock amplifier

d. Data input preamplifier and clock amplifier

e. Input preamplifiers

f. Marker output and data output driver

g. Gate-in, gate-out, and bit-counter step pulse inverters.

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Output capability in milliamperes	A	B_1	B_2	C_1	C_2	C_3	D_1	D_2	D_3
	1.3	1	0.3	2.3	3.9	2.7	2.0	0.3	3.3	1
Input requirements in milliamperes	0.4	0.16	0.7	0.6	0.66	0.38	2.3	0.04	2.3	2.3

| Output capability in milliamperes	E_1	E_2	E_3	E_4	F_1	F_2	G_1	G_2	G_3
	1	0.13	1	1	1	1	0.48	0.23	1.8
Input requirements in milliamperes	2.3	0.02	0.92	0.92	0.1	0.5	0.47	0.47	0.37

All circuits (Figure 26) except E and F are simple pulse inverting circuits. Circuits E_3 and E_4 are combined to form a gate which provides a negative output only when inputs a and c are at plus V_1 and input b is at ground. Circuit F_1 provides a positive output when either of the inputs is positive.

3.1.10.2. EQUATIONS AND CALCULATIONS. Since the equations are relatively straightforward, only the value of base current is given at the worst-case for the transistor being held on at $-20^{\circ}C$ end of life.

3.2. BIT PATH CIRCUITS

Material under the following headings describes the design of the circuitry in the bit path of the memory. The memory is operated either in a read-only mode or a write-only mode. Since the memory element is nondestructive, it is unnecessary to rewrite information during the read cycle. During a read cycle, a 16-bit word is read out of the memory, and during a write cycle a 16-bit word is written into the memory.

Figure 27 shows a partial logic schematic of the bit path circuits. There are 192 plated wires in the memory plane. There are 16 groups of read-write circuits. Thus, there are 12 plated wires in each of these 16-bit groups. Only one of the 12 plated wires in a bit group is read from or written into at a time. The selection is accomplished by the bit-sense matrix which consists of switches (represented by the dots in Figure 27) in series with the plated wires. These switches normally present a high impedance and present a low impedance only when selected by the P-counter. The P-counter determines which of the 12 bit positions will be read or written and turns on one matrix switch in each of the 16-bit groups. The design of the matrix switch will be described in the following headings.
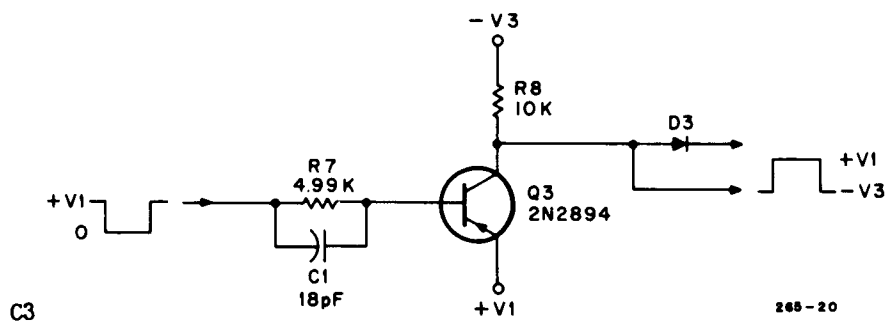
52
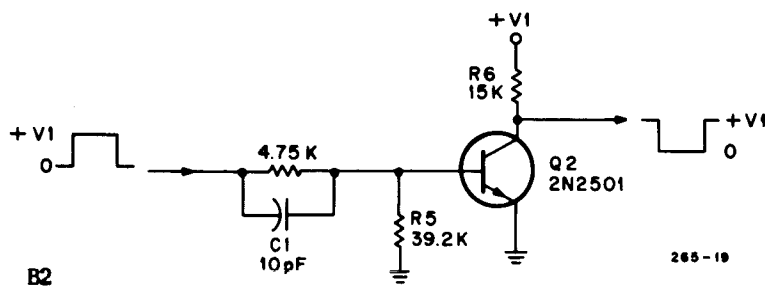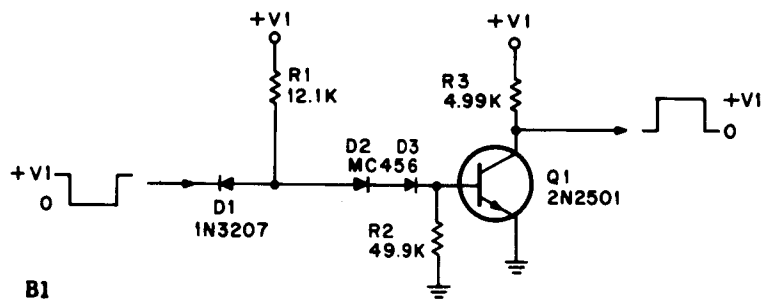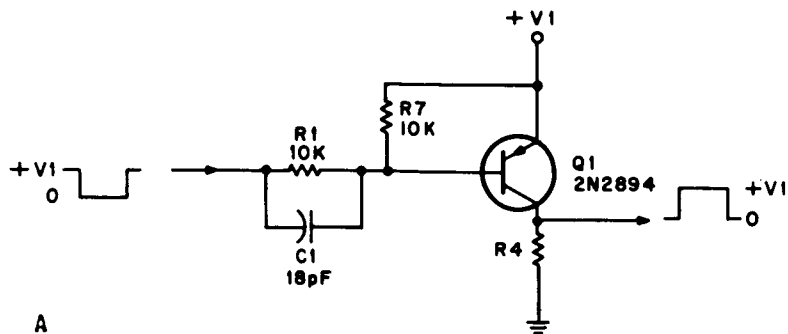
Figure 26.   Signal Inverters

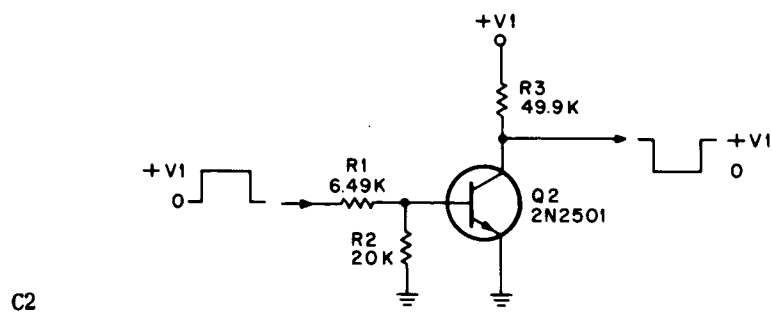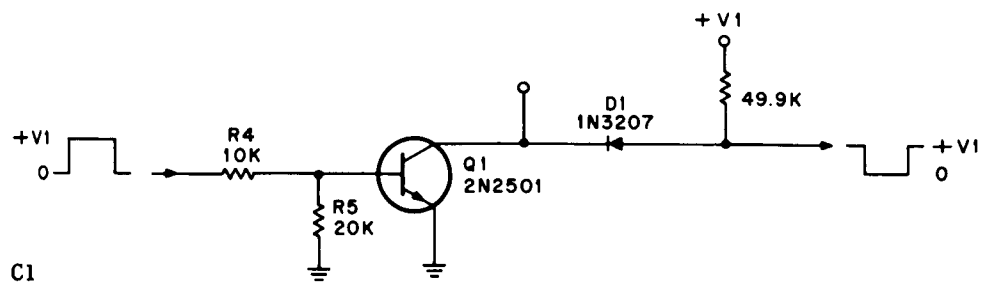Figure 26. Signal Inverters (cont)
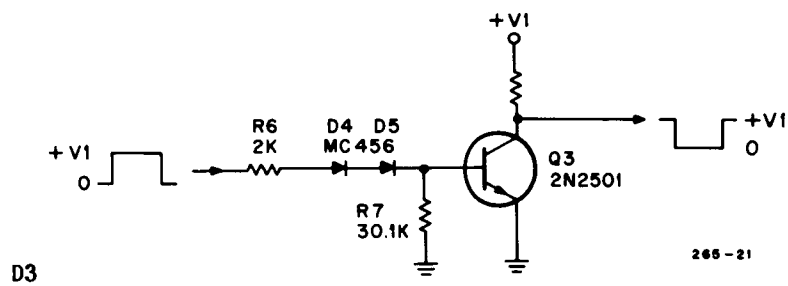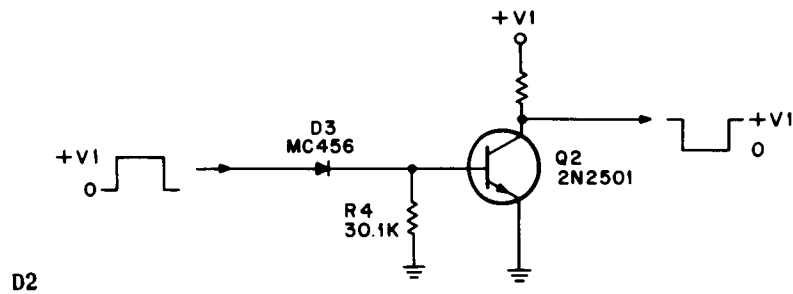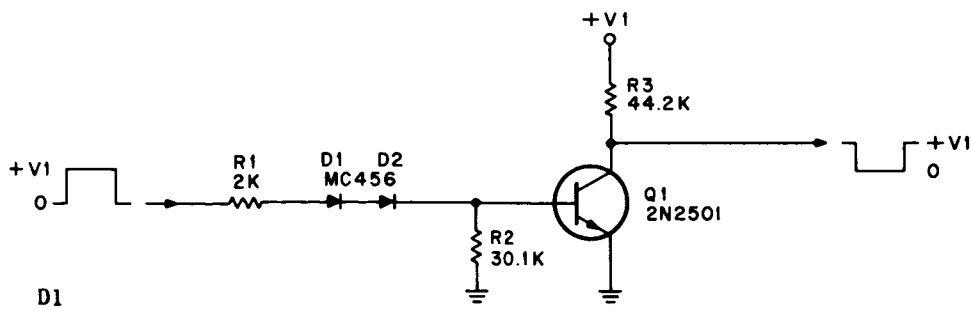
54

D1

D2

D3

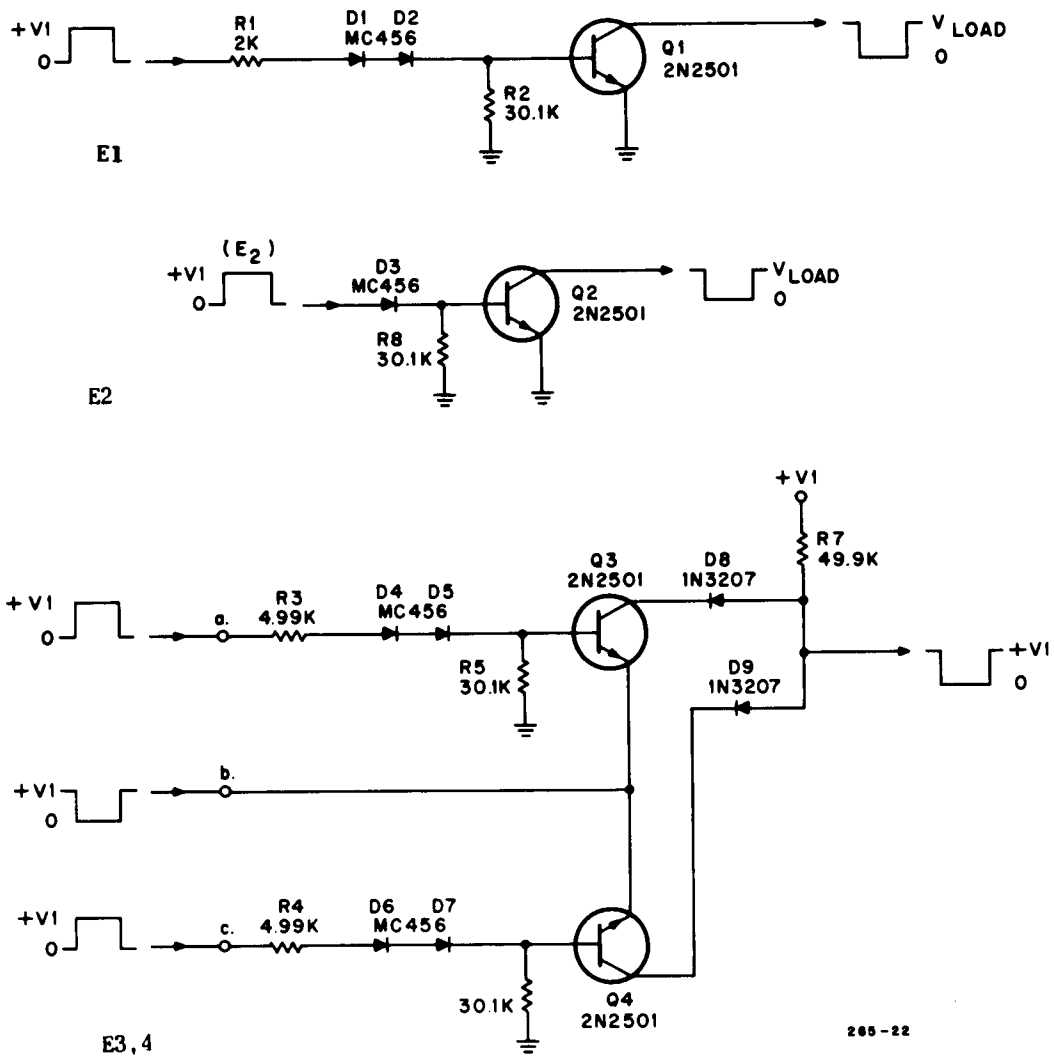Figure 26.   Signal Inverters (cont)

55

Figure 26. Signal Inverters (cont)

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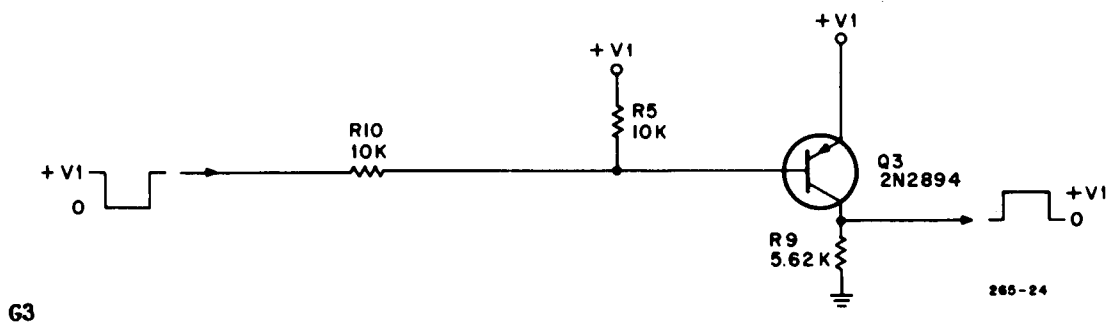Figure 26. Signal Inverters (cont)
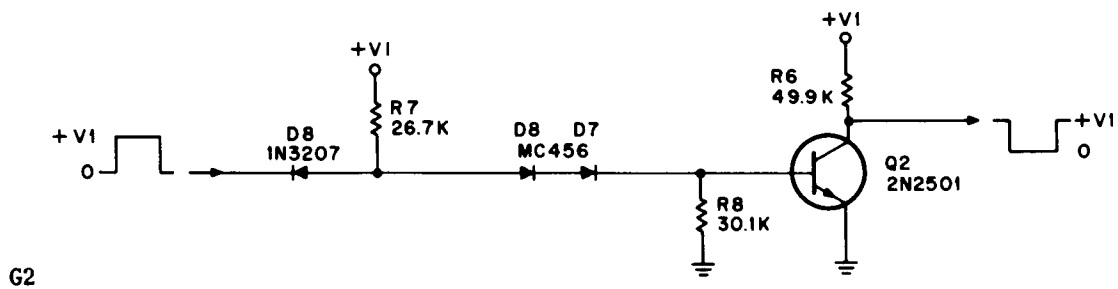
Figure 26. Signal Inverters (cont)

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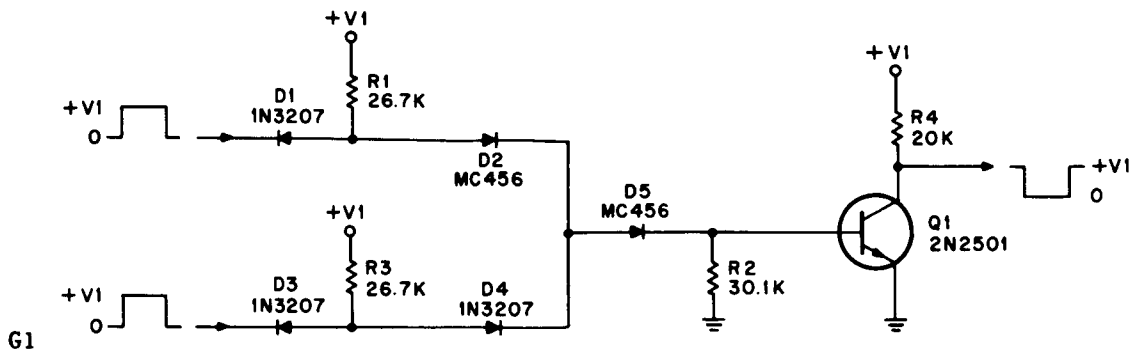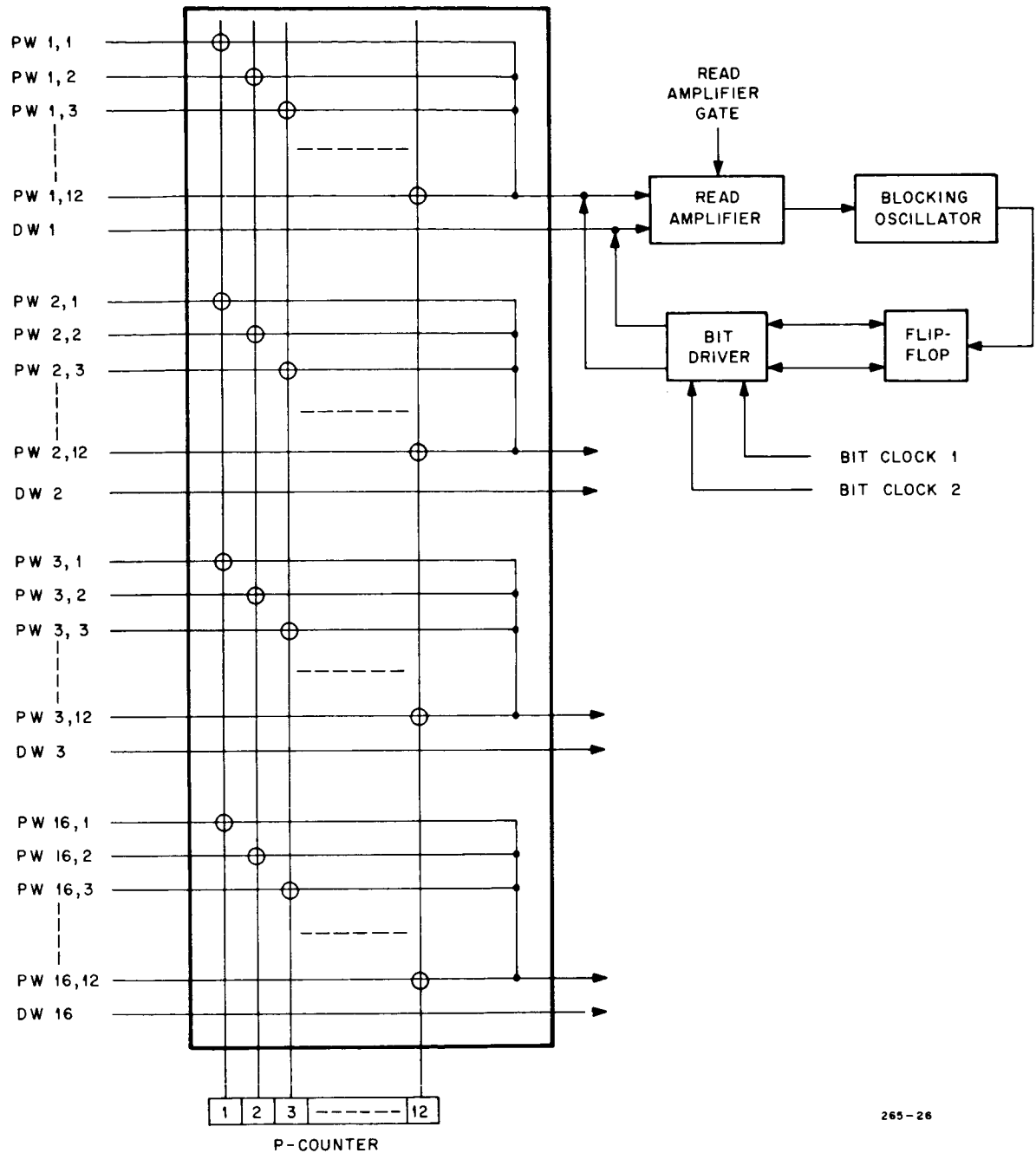Figure 27. Logic Schematic of Bit Path Circuits

During a read operation, the information flip-flop must be either set for a binary 1 or remain in the reset state for a 0. The blocking oscillator output is a negative-going pulse for a 1. The blocking oscillator is triggered by a negative output from the read amplifier, which corresponds to a positive signal from the plated wire. A positive signal from the plated wire is therefore defined as a binary 1. A binary 0 is a negative signal from the plated wire; it does not trigger the blocking oscillator, thereby leaving the information flip-flop in the reset state. The read amplifier is gated during the time a signal from the plated wire is present in the read operation. The read amplifier gate ensures that the blocking oscillator will not be triggered by noise when a signal is not present so that the flip-flop will not be set to indicate an erroneous 1. In Figure 27, the dummy wires are shown coming from the memory plane, going through the bit-sense matrix, and connecting to the read amplifier. During the read operation, the wire acts as a noise cancelling wire. The dummy wire runs parallel to the plated wires in the memory plane such that, ideally, any noise coupled into the plated wire is equally coupled into the dummy wire. The dummy wire also serves as a cancelling wire for the bit transients during a write operation to reduce the loading effect of the read amplifier on the bit current.

During a write operation, the information in the information flip-flops is written into the selected word. The bit drivers pass a current down the plated wires selected by the P-counter. If a 1 is to be written, the current waveshape is a positive pulse followed by a negative pulse, and if a 0 is to be written, the current waveshape is a negative pulse followed by a positive pulse. The timing of the double-pulse bit current is accomplished by means of the two bit clocks shown in Figure 27. Whether a 1 or 0 is written by the bit driver is determined by the logic state of the information flip-flop. The design of the bit driver is described under the following headings. Only the portion of the information flip-flop necessary to the understanding of the bit driver is described.

3.2.1. BIT-SENSE MATRIX

Specifications

The bit-sense matrix selects one out of 12 plated wires in each of the 16-bit groups to be read or written, depending on the memory operation being performed. When selected, the bit-sense matrix must therefore be capable of

either passing the bit current from the bit driver to the plated wire or passing the plated-wire signal to the read amplifier. The matrix circuits are selected identically for either a read cycle or a write cycle. The following list sets forth the basic requirements of the bit-sense matrix when selected:

Maximum small-signal impedance: 12 ohms

Maximum steady-state noise: 3 millivolts

Maximum impedance to bit current: 8.3 ohms

Maximum average power, 16 switches
on and 176 switches off: 10 milliwatts

In addition to the above requirements, the matrix circuit must present a high impedance to the bit current and to the plated-wire signals when in the unselected state.

3.2.1.1. DESCRIPTION. The matrix circuit is shown in Figure 28. One of these circuits is in series with every plated wire in the memory plane.
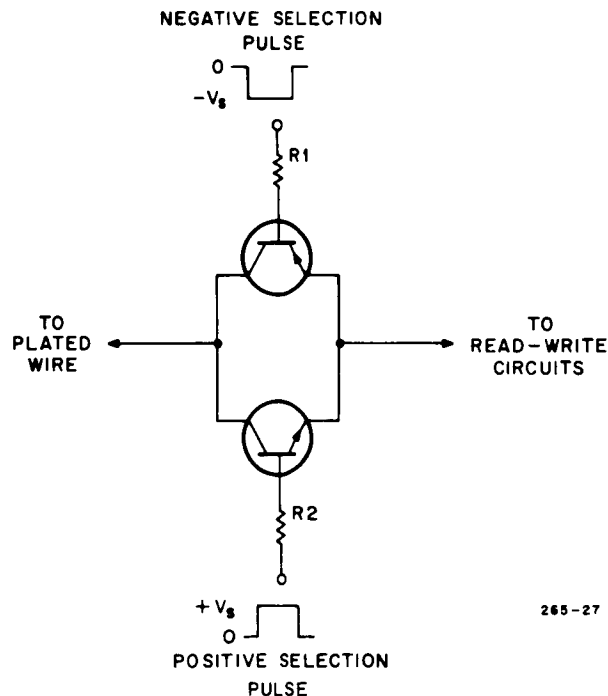

Figure 28. Bit-Sense Matrix Circuit

The emitters of the 12 pairs of transistors in a bit group are all connected together as shown in the partial circuit schematic in Figure 29. When the matrix circuit is not selected by the P-Counter, the bases of the transistors
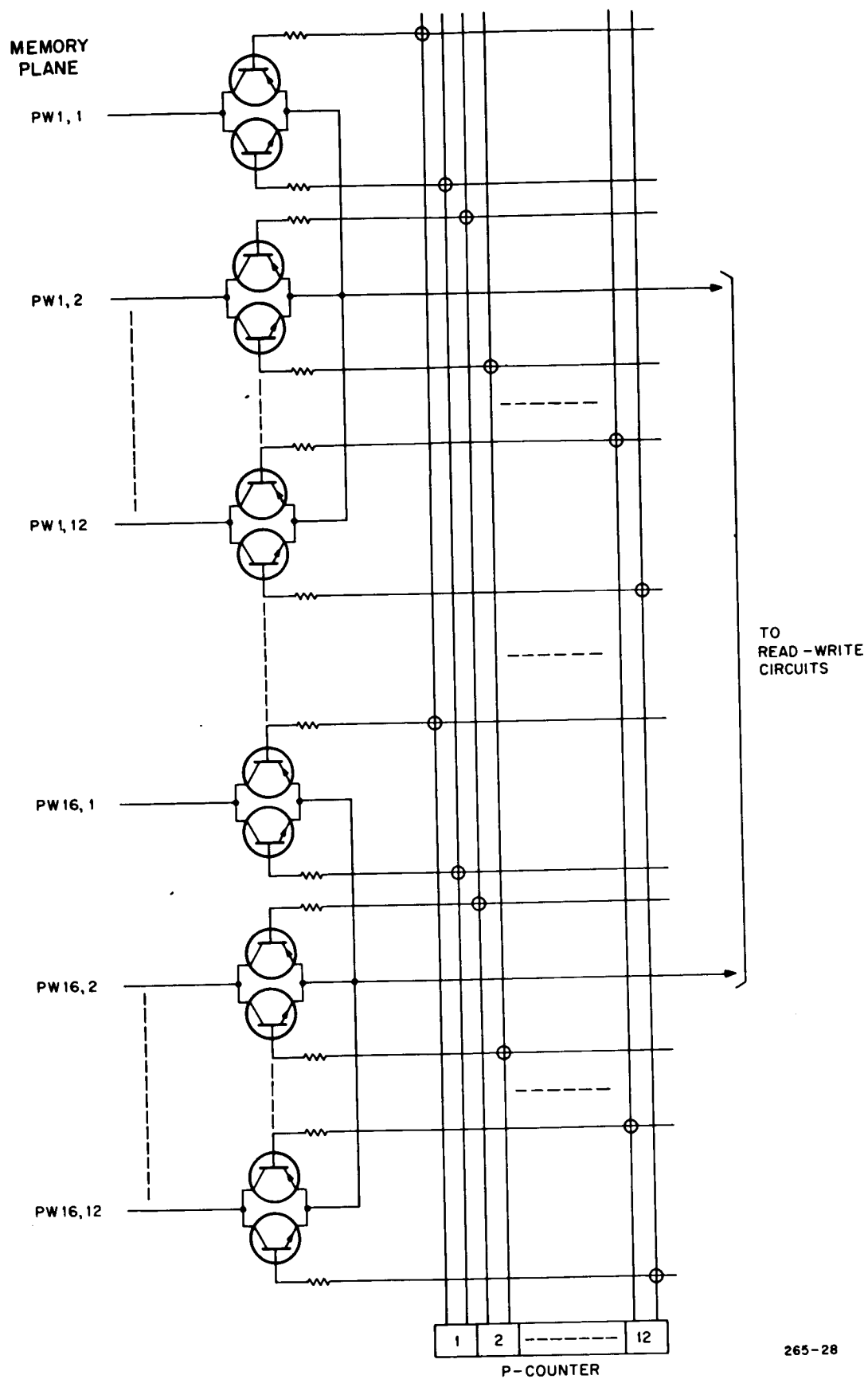
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Figure 29. Partial Schematic of Bit-Sense Matrix

are at ground potential, and there is no base current in the transistors. The matrix transistors present a resistance of several megohms in the off state to small signals from the plated wire. There is also a capacitance of a few picofarads in the off state. However, the resistance is so high and the capacitance so low that the sneak signals from the unselected plated wires during a read cycle are insignificant in comparison with the signal from the selected plated wire. In addition to presenting a high impedance to the unselected wires, the matrix circuit must not pass current from the bit driver during a write operation. The voltage which will be present at the emitter due to the bit current is determined by the impedance and length of the plated wire during the switching of the bit current and by the steady-state drop across the selected matrix circuit and its plated wire. The base-emitter drop of the matrix transistors is sufficient to hold off this volt-age. It should be noted that a matrix circuit in the off state will not pass bit current only if one of the matrix circuits in the same bit group has been selected. In the operation of the memory, however, a matrix circuit in each bit group has been selected during a write operation.

The two basic functions that a matrix circuit must perform when it has been selected are that it must pass the bit current with a low voltage drop during a write operation and it must present a low impedance to the plated-wire signal during a read operation. A matrix circuit is selected by apply-ing positive and negative balanced pulses simultaneously to the base resis-tors of Q1 and Q2, respectively, as shown in Figure 29. These pulses are supplied from the P-counter and drive a matrix circuit in each bit group. The reason for using two transistors in the circuit is to pass the bipolar bit current. The amount of base current needed for the operation of the circuit is determined by the transistor betas such that the drops across the circuit when the bit circuit is flowing will be less than or equal to the specified maximum drop. Transistor Q2 passes the positive bit current, and Q1 passes the negative bit current.

When the selection pulses are applied, practically all of the base cur-rent flows through the collectors of the transistors. The transistors, therefore, with nothing applied to the collectors or emitters are operated in the saturation region at zero emitter current. In this state, the collector-emitter characteristic is essentially a pure resistance. This is known as the saturation resistance and is defined as the slope of the

$V_{CE} - I_C$ characteristic at zero emitter current and at the specified base current. The impedance presented to the plated-wire signal due to the matrix circuit is the parallel combination of the saturation resistances of Q1 and Q2. In order for the plated-wire signal to reach the read amplifier with minimum loss, the saturation resistance of either the Q1, the Q2, or both, must be low. With the transistors used, the PNP saturation is approximately 10 times lower than that of the NPN transistors and is therefore controlling.

A brief description will now be given of the memory stack characteristics. The plated wires in their grooved ground planes form a transmission-line system. These circuits were designed for a transmission-line system two feet long. These transmission lines have an impedance of about 75 ohms, a resistance of about 1.5 ohms per foot, and a delay of about 1.7 nanoseconds per foot. The minimum switching time of the plated-wire signal is 100 nanoseconds. This switching time is so long as compared with the length of the transmission-line system that the effect of reflections of the plated-wire signal can be neglected, and the signal loss due to the transmission-line system is simply determined by the resistance of the plated wire and the dummy wire which is the return path for the signal. The transmission characteristics of the plated wire need be considered only when determining how much voltage will be present at the emitter of the unselected matrix circuits during the switching of the bit current. The calculations of this voltage are presented under heading 3.2.1.2. of this report.

The second important consideration in the design of the matrix circuit with respect to its operation during a read cycle is that it must have a low noise characteristic. The circuits are designed such that the noise generated by a selected matrix circuit is negligible when the plated-wire signal occurs. In the memory timing, the bit-sense matrix is driven by the P-counter at least 0.5 microseconds before the word current is driven. The matrix circuit and the read amplifier are therefore designed such that 0.5 microseconds after a matrix circuit is selected, the noise due to the selection is negligible. The noise generated when the matrix circuit is turned on can be considered as the sum of two components. The first component is the switching transient, which is caused primarily by unbalances of the base-emitter drops and of the base-emitter capacitances of the two transistors. This switching transient is a few millivolts in amplitude but lasts for only about 40 nanoseconds. This transient has therefore disappeared long before

the plated wire is read out. The second component of the matrix noise is a steady-state voltage which is caused by the selection current flowing through the matrix transistors. Since the saturation resistance of the NPN transistor is much larger than that of the PNP transistor, the emitter-offset voltage of the PNP transistor is the steady-state voltage caused by the selection of a matrix circuit. The emitter-offset voltage is defined as the emitter-collector voltage at zero emitter current and at the specified base current. In addition to the transistor offset voltage, there is the possibility that a steady-state voltage will exist because of an unbalance in the selection current. This unbalance current flows down the plated wire, and the voltage is due to the resistive drop in the plated wire. The unbalance current is caused by unbalances in the base resistors and in the base-emitter drops of the transistors. Altogether, a steady-state voltage of three millivolts can exist when a matrix circuit is selected.

As will be shown under heading 3.3. of this report, the input to the amplifier has a 0.152-microsecond time constant because of the small coupling and signal-bypass capacitors. Therefore, after 0.5 microseconds, or three time constants, the three-millivolt steady-state voltage has decayed in the amplifier to an equivalent 0.12 millivolts at the input. It should be noted that the steady-state voltage is always negative in polarity and is therefore in the same direction as the 1 signal. The equivalent amplitude of the matrix noise of 0.00 to 0.12 millivolts during the time the plated-wire occurs means that 0.12 millivolts of the positive signal, or a 0, is required to overcome the matrix noise. This is due to the fact that to ensure that the blocking oscillator does not trigger in the presence of a 0, the sum of the 0 signal and any noise present must be equal to or more positive than zero. A more detailed analysis of the plated-wire signal requirements is given in the section of this report describing the design of the read amplifier.

3.2.1.2. CIRCUIT DESIGN. The NPN transistor used in the matrix circuit is the standard logic transistor, XT-169, used throughout the rest of the memory. The PNP transistor characteristics are set forth in transistor specification XT-181. Standard derating procedures are used in the design of the matrix circuit.

The amount of selection current required by the matrix circuit is determined by the amount of bit current the matrix transistors must pass. The

amount of base current supplied to the matrix transistor Q1 in worst-case is as follows:

$$I_{b1} = \frac{V_s - \overline{V_{be1}}}{\overline{R1}}$$ (15)

Substituting and solving

$$I_{b1} = \frac{5.0 - 1.0}{(1.03)(1.74 \times 10^3)} = 2.25 \text{ milliamperes}$$

The matrix circuit is designed to pass a bit current of 30 milliamperes. The minimum circuit beta of the matrix is therefore:

$$B_{CCT} = \frac{30 \times 10^{-3}}{2.25 \times 10^{-3}} = 13.3$$

The minimum transistor beta is 35 at beginning of life. Allowing 50 percent derating for life and 20 percent for temperature, the worst-case end-of-life transistor beta is 14.0, which is greater than that required. The minimum base current and beta requirements to transistor Q2 are identical to those of transistor Q1.

The matrix transistors are specified to have a maximum V_{CE} drop of 0.20 volts. Derating this by 20 percent, the maximum steady-state voltage drop across the selected matrix switch when the bit current is flowing is 0.25 volts. In addition to this, 0.10 volts is developed due to the resistive drop of the plated wire. The unselected matrix transistor therefore must present a high impedance during the steady-state bit current to 0.35 volts. The base-emitter drop of the transistors alone is sufficient to present a high impedance to the steady-state bit current, and the unselected transistors do not need to be reverse-biased.

During the rise time of the bit current, a transient voltage is developed at the input to the plated wire as given by:

$$V_T = \frac{I_{bit} \, Z_{ob} \, 2\Delta}{T_R} \qquad (16)$$

where Z_{ob} is the impedance of the bit wire, T_R is the rise time of the bit current, and Δ is the total one-way delay between the grounded end of the bit wire and the bit driver. Substituting and solving:

$$V_T = \frac{30 \times 10^{-3} \times 75 \times 8 \times 10^{-9}}{60 \times 10^{-9}} = 0.3 \text{ volts}$$

During the switching of the bit current, therefore, a maximum voltage of 0.65 volts will appear at the input to the unselected matrix switches for the assumed 60-nanosecond rise time of the bit current. At this voltage, the unselected matrix transistors will conduct some of the bit current, and the result is that the rise time of the bit current is limited to about 75 nanoseconds.

The requirement that the matrix present a low impedance to the plated-wire signal is met by specifying a maximum of 15 ohms at 1.5 milliamperes of base current for the saturation resistance of the PNP transistor. Since the saturation resistance is inversely proportional to base current, the maximum saturation resistance at the minimum base current is 10 ohms at beginning of life. This is derated by 20 percent to give an end-of-life saturation resistance of 12 ohms.

The matrix offset requirement is met by specifying a maximum of 2.5 millivolts at two milliamperes of base current for the emitter offset.

The maximum power required by the 16 matrix switches selected in parallel is:

$$\overline{P_M} = 16 \times \frac{\overline{V_s} - V_{bE}}{\underline{R}} \times 2\overline{V_s} \times \frac{\overline{T_M}}{\underline{T_R}} \qquad (17)$$

where T_M is the time the matrix is on in a memory cycle, and T_R is the time between memory cycles. Substituting and solving:

$$\overline{P}_M = 16 \times \frac{5.9 - 0.6}{(0.97)(1.74 \times 10^{+3})} \times (2)(5.9) \times \frac{2.5 \times 10^{-6}}{160 \times 10^{-6}}$$

or, $\overline{P}_M = 9.3$ milliwatts

3.2.2. READ AMPLIFIER

Specifications

The only functional requirement of the read amplifier is to amplify a binary 1 signal from the plated wire to an amplitude sufficient to trigger the blocking oscillator which, in turn, sets the information flip-flop. The gain of the read amplifier is expressed in terms of conductance since the input signal is a voltage source and the output stage is a current source. Because of the nonlinearity and limited frequency response of the amplification stages, the conductance is determined for the actual output current required and for the fastest switching time of the input signal to the memory. The second read amplifier stage is gated to the output of the amplifier to provide an output current large enough to trigger the blocking oscillator during the time the gate signal is present. The input to the read amplifier senses only differential signals so that common-mode noise on the input is rejected. The time constant of the read amplifier input stage causes the d-c offset of the bit-sense matrix to decay in the amplifier to a low value by the time the plated-wire signal occurs. The following is a list of the circuit characteristics:

Input—

    Rejects common-mode signals

    Maximum time constant: 0.15 microsecond

    Minimum 1 signal: 3.0 millivolts

    Minimum small-signal input impedance: 130 ohms

    Minimum switching time of 1 signal: 100 nanoseconds

Output—

    Minimum amplitude for 1 signal when gated: 140 microamperes

    Minimum amplifier conductance: 0.047 mhos

Gate Signal—

> Voltage when off: Ground
> Minimum signal voltage: 4.5 volts
> Minimum input current: 9.2 milliamperes
> Pulse width: 100 ±10 nanoseconds

Maximum Power: 2.0 milliwatts

The minimum 1 signal given above is the amount of signal voltage which must appear at the input terminals of the read amplifier to provide the required output signal. This is not the plated-wire signal required because the effects of losses and differential noise must be considered to determine this signal. The amount of plated-wire 1 signal required in the absence of any noise is 3.5 millivolts; this figure includes losses in the signal transmission to the amplifier input. Any noise at the input increases the amount of signal required. The plated-wire 0 signal must only be large enough to overcome any differential noise.

3.2.2.1. DESCRIPTION. The read amplifier is shown in Figure 30. The input transformer provides a 5:1 voltage step-up ratio. One of the inputs to the transformer is the output of the bit-sense matrix which supplies the signal to be amplified from the selected plated wire. The other input to the input transformer is the dummy wire which provides word-noise cancellation. Ideally, any noise coupled to the plated wire is also coupled to the dummy wire. The net voltage appearing across the input winding of the input transformer due to the word noise is therefore zero and does not appear on the secondary winding. Thus, the input transformer couples only differential signals to the secondary winding. The 5:1 voltage step-up windings are part of the AT-3 transformer.

Transistors Q1 and Q2 are class-A biased to amplify the plated-wire signal. The collector supply for transistor Q2 is in the blocking oscillator module (resistor R1 in Figure 31). Resistors R3, R4, R5, and R6 provide the biasing voltage for transistor Q1. Capacitors C1 and C3 provide d-c isolation for the biasing voltage. Resistors R7, R8, and R9 determine the biasing voltage of transistor Q2. During a write cycle, a voltage transient will appear on the secondary of the input transformer. Resistor R2 provides an impedance to the bit transient which is high compared to the impedance of the desired current path through the bit-sense matrix to the plated wire.
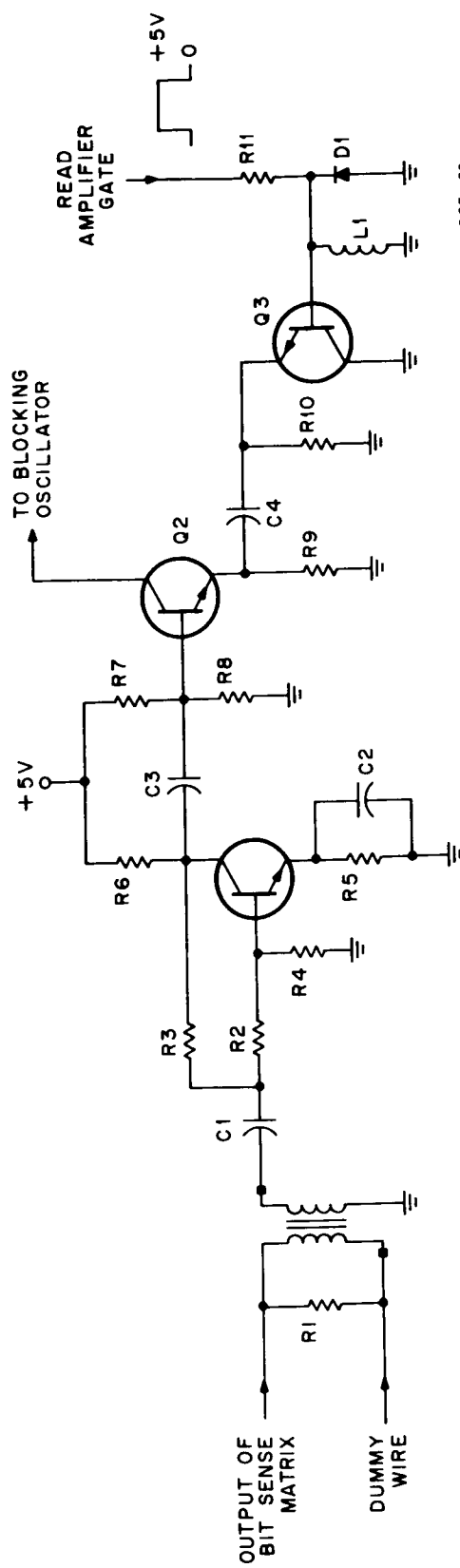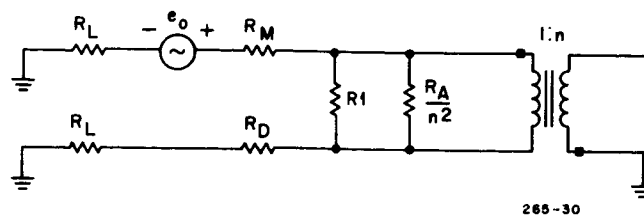
Figure 30. Read Amplifier

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Figure 31. Equivalent Circuit of
Read Amplifier

Without R2, a positive bit transient on the secondary of the input transformer would turn transistor Q2 on and saturate it. With C1 and C2 acting as bypass capacitors, the voltage on the secondary of the input transformer would become clamped by the base-emitter diode of Q1, the effect of which would be to degrade the rise time of and the tolerance of the bit current. Resistor R2 therefore presents a high impedance to the bit transient but a low impedance compared to the normal input impedance of Q2 so that the amount of signal loss across it is small.

When the bit-sense matrix is selected, a d-c offset voltage appears on the input to the read amplifier. This offset voltage is comparable to the plated-wire signal voltage and cannot be allowed to be amplified when the plated-wire signal occurs. The input stage of the read amplifier is therefore designed such that the a-c-coupled offset voltage decays to a small value in the amplifier by the time the readout of the plated wire occurs. This is accomplished by making the time constant of the input stage small and by making the emitter bypass capacitor C2 small; C2 is made large enough, however, to present a low impedance to the plated-wire signal. Capacitors C1, C3, and C4 are also large enough to present a low impedance to the signal.

Except when the plated-wire signal is present, the amount of current that the read amplifier can supply to the blocking oscillator must be limited to a small value such that the blocking oscillator will not be triggered. In other words, the ratio of the gain when the readout occurs to the gain during all other times must be very high. This is accomplished by gating the emitter of transistor Q2. When the read amplifier gate is at the ground state, transistor Q2 is off, and the emitter impedance is the parallel combination of resistors R9 and R10, both of which are large. Resistor R10 provides a recovery path to ground for capacitor C4 when transistor Q3 is

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off. When the read amplifier gate is applied, transistor Q3 is turned on to a low impedance by means of the gate current flowing through the base-collector junction. This provides a low-impedance path in the emitter of transistor Q2, and the amplifier gain is increased accordingly. The noise generated by the gate is merely the emitter offset voltage of Q3, which is so low in comparison with the amplitude of the plated-wire signal in this stage of the amplifier that it can be neglected. Inductor L1 provides clean-up current to the base of gate transistor Q3 during the turn-off of the gate. Initially, all of the gate current flows into the base of Q3. The current in L1 increases linearly since the voltage across it is clamped by the base drop of Q3. The value of L1 is chosen such that there is still enough base current at the end of the gate time for Q3 to present a low impedance. Diode D1 provides a recovery path for the current in inductor L1 to clamp the base of Q3 at the voltage drop of D1 for the duration of the recovery of L1.

The amplifier must amplify a 1 signal such that the output current is large enough to trigger the blocking oscillator. There is no amplification required for a 0. The primary problem in the design of the read amplifier was to achieve the amount of gain required to amplify a memory 1 without dissipating any more power in the amplification stages than necessary. A 1 at the base of transistor Q1 is a negative signal and tends to turn Q1 off. Transistor Q1 is therefore biased at a current level that does not cause the input impedance to be increased significantly by the signal. Because of the high impedances in the collector circuit of Q1, the frequency response of the first stage is very limited, but to achieve a significantly lower imped-ance would require excessive power dissipation. A 1 at the base of the sec-ond amplifier transistor Q2 is a positive signal and turns Q2 on to a higher collector current. Transistor Q2 is therefore biased at a lower current than Q1, and advantage is taken of the fact that the gain of Q2 becomes higher when the signal is applied.

The amount of 1 signal required is the sum of any noise present at the input plus that required to trigger the blocking oscillator. The 0 signal required should be low enough so that no current is delivered to the block-ing oscillator by the read amplifier.

3.2.2.2. CIRCUIT DESIGN. The specification for the amplifier transistors Q1 and Q2 are set forth in transistor specification XT-180. The specifica-tions for the gate transistor Q3 are set forth in transistor specification

XT-179. Diode D1 is a 1N-3207. Unless otherwise noted, standard derating procedures are employed in the design of the read amplifier. The following is a list of the component values used in the read amplifier:

Component	Value	Units
R1	500	ohms
R2	1.00	K ohms
R3	51.1	K ohms
R4	300	K ohms
R5	5.90	K ohms
R6	10.0	K ohms
R7, R8, R9, R10	100	K ohms
R11	374	ohms
C1	680	picofarads
C2	680	picofarads
C3	1000	picofarads
C4	1000	picofarads
L1	15.0	microhenries

The gain of the read amplifier is practically constant for temperature variation. The primary reason for this is that at the low bias currents employed, the transistor impedance levels are so high that the voltage gain of the first transistor stage is primarily determined by the frequency response of that stage. The reason for the frequency limitation is the gain degeneration caused by the collector-to-base capacitance of transistor Q1. With a high impedance in the collector (due to the high input impedance of transistor Q2), the voltage gain of the first stage is fairly high at low frequencies, but the effective collector-to-base capacitance, which is the actual collector-to-base capacitance times one, plus the voltage gain, is high enough such that at the frequencies being amplified the variations of the input impedance of the first stage are negligible. The gain of the second stage is expressed in terms of conductance because its input, the output of the first stage, is essentially a voltage source at the frequencies being amplified and because the required output is expressed in terms of current. The capacitances of transistor Q2 do present some frequency limitation on the signal amplification, but these can be considered as part of the frequency limitation on the voltage gain of the first stage. The conductance of the second stage can then be determined by knowing the transistor impedance and the saturation resistance of gate transistor Q3. The input impedance is directly proportional to the temperature. The conductance of the second stage therefore decreases with an increase of temperature, but the

decrease is stabilized to some degree by an increase of bias current due to a decrease in the base-emitter voltage drop. The gain of the amplifier is thus determined at the highest temperature because the gain is the lowest at that temperature and because the worst-case current requirement for the blocking oscillator also occurs at the highest temperature. The amount of output current required is 140 microamperes. The common-base input impedance of Q2 is derated five percent for life and at 50°C. The maximum common base input impedance h_{ib2} is

$$\overline{h_{ib2}} = \frac{28.5 \times 10^{-3}}{I_{E2} + i_{e2}} \tag{18}$$

where $I_{E2} + i_{e2}$ is the total emitter current of transistor Q2. The change of base-emitter voltage for a change of emitter current is given by:

$$\frac{d \ v_{be2}}{d \ i_{e2}} = h_{ib2} \tag{19}$$

The preceding two equations can be combined to find the change of base-emitter voltage v_{be2} for a change of emitter current i_{e2}:

$$v_{be2} = 28.5 \times 10^{-3} \ \ln \frac{i_{e2} + I_{E2}}{I_{E2}} \tag{20}$$

where I_{E2} is the initial emitter current which is the bias current of transistor Q2 and is expressed by

$$I_{E2} = \frac{V_{CC} - V_{bE2} \ \frac{R7 + R8}{R8}}{\frac{R7}{H_{FE2} + 1} + \frac{R9(R7+R8)}{R8}} \tag{21}$$

where V_{CC} is the 5-volt supply voltage, V_{bE2} is the base-emitter drop, and H_{FE2} is the d-c common-emitter current gain. The conductance of the second stage is

$$g_2 = \frac{i_{c2}}{v_{b2}} \quad \text{where} \tag{22}$$

$$v_{b2} = v_{be2} + i_{e2}\, r_3 \tag{23}$$

where r_3 is the saturation resistance of the gate transistor Q3. The lowest conductance occurs when the bias current is minimum.

$$I_{E2} = \frac{V_{CC} - \overline{V_{bE2}}\, \dfrac{\overline{R7} + \underline{R8}}{\overline{R8}}}{\dfrac{\overline{R7}}{H_{FE2} + 1} + \dfrac{\overline{R9}(\overline{R7} + \underline{R8})}{\underline{R8}}} \tag{24}$$

Substituting and solving

$$I_{E2} = \frac{4.8 - 0.69 \dfrac{103 + 97}{97}}{\dfrac{103}{15 + 1} + \dfrac{103(103 + 97)}{97}} \times 10^{-3} = 16.0 \text{ microamperes} \tag{25}$$

V_{bE} has been derated only 10 percent since the transistor is being operated in class–A mode so that the base-emitter drop is stabilized; H_{FE} has only been derated 40 percent for the same reason. To obtain an output current, i_{e2}, of 140 microamperes in worst-case

$$i_{e2} = \frac{H_{FE2} + 1}{H_{FE2}}\, i_{c2} = \frac{15 + 1}{15}\, 140 \text{ microamperes} = 149 \text{ microamperes} \tag{26}$$

The d-c current gain was used in the preceding equation for ease of specifying the transistor. The small-signal current gain is somewhat higher. Substituting the worst-case values into equation (20)

$$\overline{v_{bE2}} = 28.5 \times 10^{-3} \ln \frac{149 + 16.0}{16.0} = 66 \text{ millivolts} \tag{27}$$

From equation (23) the worst-case signal swing at the base of transistor Q2 is

$$\overline{v_{b2}} = \overline{v_{be2}} + \underline{i_{c2}}\ \overline{r_{s3}} \tag{28}$$

$$= 66 - 10^{-3} + 149 \times 10^{-6} \times 50$$

$$= 7.35 \text{ millivolts}$$

The worst-case conductance of the second stage is therefore

$$\underline{g_2} = \frac{\underline{i_{c2}}}{\overline{v_{b2}}} = \frac{140 \times 10^{-6}}{72.5 \times 10^{-3}} = 1.91 \times 10^{-3} \tag{29}$$

The voltage gain of the first stage of the amplifier is lowest at the lowest bias current. The minimum collector current of transistor Q1 is given by

$$\underline{I_{c1}} = \frac{\underline{V_{CC}} - \overline{V_{bE1}}\left(\dfrac{\overline{R2}+\overline{R3}+\underline{R4}+\overline{R6}}{\underline{R4}}\right)}{\overline{R6} + \dfrac{\overline{R2}+\overline{R3}+\overline{R6}}{\underline{H_{FE1}}} + \dfrac{(\underline{H_{FE1}}+1)(\overline{R5})(\overline{R2}+\underline{R3}+\underline{R4}+\overline{R6})}{\underline{H_{FE1}} \times \underline{R4}}} \tag{30}$$

where $\overline{V_{bE1}}$ is the base-emitter voltage drop and H_{FE1} is the minimum d-c common-emitter current gain. Both of these parameters are derated the same as for transistor Q2. Substituting and solving

$$\tag{31}$$

$$\underline{I_{c1}} = \frac{4.8 - 0.69\ \dfrac{1.03 + 52.8 + 293 + 10.3}{293}}{10.3 + \dfrac{1.03 + 52.8 + 10.3}{15}\quad \dfrac{16 \times 6.09 \times (1.03+52.8+293+10.3)}{15 \times 293}} \times 10^{-3}$$

or $\underline{I_{c1}} = 175$ microamperes.

The voltage gain of the first stage was measured with the worst-case transistors under worst-case loading and biasing conditions, and to a half sine wave with an 80-nanosecond base the voltage gain, a_{v1}, was measured to be 5.5.

The 80-nanosecond base was used because it represents the highest frequencies that must be amplified. The worst-case conductance of the two transistor stages is therefore

$$\underline{g_{12}} = 5.5 \; \underline{g_2} = 5.5 \times 1.91 \times 10^{-3} = 10.5 \times 10^{-3} \tag{32}$$

The overall conductance of the amplifier is determined by including the voltage step-up of the input transformer. Because of the transformer capacitance, the voltage step-up of the input transformer is only 4.5 at the frequency being amplified. The overall conductance of the amplifier, g_a, is therefore

$$\underline{g_a} = 4.5 \; g_{12} = 4.5 \times 10.5 \times 10^{-3} = 47.2 \times 10^{-3} \tag{33}$$

The amount of plated-wire signal at the input of the amplifier given an output current of 140 microamperes is

$$e_s = \frac{\underline{i_{c2}}}{\underline{g_a}} = \frac{140 \times 10^{-6}}{47.2 \times 10^{-3}} = 2.96 \text{ millivolts} \tag{34}$$

To determine the amount of plated-wire signal required to operate the amplifier, the losses in the signal path must be considered. An equivalent circuit of the signal path is shown in Figure 31, where R_L is the resistance of the plated wire, R_M is the resistance of the bit-sense matrix, R_A is the input impedance of the read amplifier as viewed from the secondary of the input transformer, and R_D is a resistor in series with the dummy wire to provide a balanced-bit transient. The input impedance of the amplifier is approximately the sum of R2 and the input impedance of transistor Q1:

$$R_A = R2 + h_{fe1} \; h_{ib1} \tag{35}$$

where h_{fe1} is the a-c common emitter current gain. Worst-case conditions occur when the input impedance is minimum and the series resistances are maximum.

$$R_A = R2 + h_{fe1} h_{ib1}$$

or   (36)

$$R_A = 970 + (20)(130) = 3570 \text{ ohms}$$

The effective input impedance is the parallel combination of R1 and R_A/n^2.

$$R_{in} = \frac{R1 \, R_A}{n^2 R1 + R_A} = \frac{(485)(3570)}{(4.5)^2(485) + 3570} = 130 \text{ ohms} \qquad (37)$$

The amount of plated-wire signal, e_o, required is

$$e_o = e_o \frac{2R_L + R_M + R_D + R_{in}}{R_{in}} = 2.96 \frac{9 + 12 + 4 + 130}{130} \qquad (38)$$

or $e_o = 3.5$ millivolts.

This latter figure represents the amount of signal required to sense a 1 in the absence of any noise. The amount of noise present at the input to the amplifier must be included to determine the actual amount of 1 signal required. The amount of 0 signal required is only the amount necessary to overcome the noise at the input of the amplifier for a net input of zero for a binary 0.

Three requirements were considered in the design of the gate circuit. The first is that the impedance of transistor Q3 be high when the gate is off. The impedance of Q3 is several megohms and is so high in comparison to the parallel combination of resistors R9 and R10 that the latter is the impedance at the emitter of transistor Q2. The values of resistors R9 and R10 are, in turn, so high that the only effective current path to the blocking oscillator is through the collector-base capacitance of transistor Q2. This capacitance is low enough so that only the large bit transients can sneak through to trigger the blocking oscillator, and, as will be seen in the description of the bit driver, this causes no problems. The second gate circuit requirement is that it must present a low collector-emitter impedance when the gate signal is applied. The saturation resistance of the gate

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transistor decreases as the base current is increased. The base current will be at its lowest value at the end of the gate signal because the current in inductor L1 is greatest at this time. The minimum input current from the gate pulse is

$$I_G \pm \frac{V_G - \overline{V_{bc}}}{\overline{R11}} = \frac{4.5 - 0.95}{385} = 9.2 \text{ milliamperes} \qquad (39)$$

The maximum current in the inductor after 100 nanoseconds, the minimum gate width, is

$$\overline{I_L} = \frac{\overline{V_{bc}} \, \underline{I_G}}{\underline{L1}} = \frac{0.95 \times 100 \times 10^{-9}}{12 \times 10^{-6}} = 7.9 \text{ milliamperes} \qquad (40)$$

which means that in worst-case operation there is over one milliampere of base current. The maximum saturation resistance is specified as one milliampere of base current, and, therefore, the resistance of the gate will be less than the specified resistance for the duration of the gate pulse. The final consideration in the design of the gate is the noise generated by it. When the gate is on, the noise is merely the d-c emitter offset of the gate transistor. This is specified to be so low in comparison with the required signal voltage that it is negligible. When the gate is turned off, current is capacitively coupled to the output of the read amplifier through the base-collector capacitance of the gate transistor when the base voltage swings negative. The base-collector capacitance is a low value to prevent the current coupled to the blocking oscillator from triggering it.

The final consideration in the design of the read amplifier is the time constant of the input stage. This time constant is determined by the series of resistances and capacitances in the input path; namely, C1, C2, R2, and the input impedance of Q1. The time constant is expressed as

$$RC_{IN} = [R2 + h_{ib1}(h_{fe1}+1)] \left[\frac{C1 \, C2}{C1(h_{fe1}+1) + C2}\right] \qquad (41)$$

The offset voltage appears as a step function at the input and will decay in the amplifier with a time constant as expressed in equation (39). The maximum voltage in the amplifier caused by the offset during the time the plated-wire signal is amplified will occur when this time constant is maximum.

$$\overline{RC_{IN}} = [\overline{R2} + \overline{h_{ib1}}(h_{\underline{fe1}}+1)] \left[\frac{\overline{C1}\ \overline{C2}}{\overline{C1}(h_{\underline{fe1}}+1) + \overline{C2}}\right] \tag{42}$$

Substituting the worst-case values and solving

$$\overline{RC_{IN}} = [1030 + 163(20+1)] \left[\frac{(750)(750)}{750(20+1) + 750}\right] \times 10^{-12} \tag{43}$$

$$= 0.53 \text{ microseconds.}$$

The bit path circuits are designed to read out the memory information 0.5 microseconds after the selection of the bit-sense matrix by the P-counter. The matrix noise at this time is

$$\overline{N_M} = \overline{V_M} e^{-0.5/0.152} \tag{44}$$

where $\overline{V_M}$ is the maximum matrix offset. The effective matrix noise is therefore

$$\overline{N_M} = 3.0 \times 10^{-3} e^{-0.5/0.152} = 0.11 \text{ millivolts} \tag{45}$$

3.2.2.3. POWER REQUIREMENTS. There is no power supply filtering required by the read amplifier because resistors R6 and R7 are large enough to isolate any transients in the power supply. The amount of power required by the read amplifier is determined by the current drawn from the five-volt supply to bias transistors Q1 and Q2 and by the average current supplied to the read amplifier gate. The bias power in the first stage is

$$P_1 = \frac{V_{CC}\ (V_{CC}-V_C)}{R6} \tag{46}$$

where V_C is the voltage at the collector of Q1 as expressed by

$$V_C = \frac{V_{CC} + \frac{R6}{R5} V_{bE1}}{1 + \frac{R6(R4+R5)}{R5(R2+R3+R4)}} \qquad (47)$$

The worst-case power occurs when V_{CC} is a maximum and V_C is a minimum, which corresponds to the largest amount of current being drawn from the supply.

$$\underline{V_C} = \frac{\overline{V_{CC}} + \frac{R6}{R5} V_{bE1}}{1 + \frac{\underline{R6}(\overline{R4}+\underline{R5})}{\underline{R5}(\underline{R2}+\underline{R3}+\overline{R4})}} \qquad (48)$$

substituting the worst-case values and solving

$$\underline{V_C} = \frac{5.2 + \frac{9.7}{5.72} 0.50}{1 + \frac{9.7}{5.72} \frac{309 + 5.72}{0.97 + 49.5 + 309}} = 2.44 \text{ volts} \qquad (49)$$

The maximum power in the first stage is therefore

$$\overline{P_1} = \frac{\overline{V_{CC}}(\overline{V_{CC}} - \underline{V_C})}{\underline{R6}} = \frac{5.2(5.2 - 2.44)}{9.7 \times 10^{-3}} = 1.48 \text{ milliwatts} \qquad (50)$$

The bias power required by the second stage is

$$P_2 = V_{CC} \left[\frac{V_{CC}}{R7 + R8} \left(1 + \frac{R8}{R9}\right) - \frac{V_{bE2}}{R9} \right] \qquad (51)$$

The worst-case equation for the second-stage bias power is

$$\overline{P_2} = \overline{V_{CC}} \left[\frac{\overline{V_{CC}}}{\underline{R7} + \overline{R8}} \left(1 + \frac{\overline{R8}}{\underline{R9}}\right) - \frac{V_{bE2}}{\underline{R9}} \right] \tag{52}$$

Substituting the worst-case values and solving

$$\overline{P_2} = 5.2 \left[\frac{5.2}{97 + 103}\left(1 + \frac{103}{97}\right) - \frac{0.5}{97} \right] \times 10^{-3} \tag{53}$$

$$\overline{P_2} = 0.30 \text{ milliwatt}$$

This latter figure includes the power dissipated by the collector supply resistor which is located in the blocking oscillator module.

The average power dissipated in the gate circuit is

$$P_G = V_G \frac{V_G - V_{bC}}{R11} \frac{T_G}{T_R} \tag{54}$$

where T_G is the width of the gate pulse and T_R is the time between cycles. The maximum gate power is

$$\overline{P_G} = \overline{V_G} \frac{\overline{V_G} - \underline{V_{bC}}}{\underline{R11}} \frac{\overline{T_G}}{\underline{T_R}} \tag{55}$$

Substituting the worst-case values and solving

$$\overline{P_G} = 5 \frac{5 - 0.61}{363} \frac{112}{160} = 0.04 \text{ milliwatt} \tag{56}$$

The maximum power required by the read amplifier is the sum of the maximum power calculated above.

$$\overline{P} = \overline{P_1} + \overline{P_2} + \overline{P_G}$$

or   (57)

$$\overline{P} = 1.48 + 0.30 + 0.04 = 1.82 \text{ milliwatts}$$

As can be seen from the above figures, most of the power required by the read amplifier is dissipated in the biasing of the first stage. The relatively high bias current is necessary to maintain the first-stage gain to the 1 signal as explained previously.

3.2.3. BLOCKING OSCILLATOR

Specifications

The blocking oscillator amplifies the low-level output of the read amplifier to provide a signal capable of driving logic circuits. In addition to amplifying the output level of the read amplifier, the blocking oscillator provides an output pulse whose width is greater than that of the input. This is required because a signal whose width corresponds to that of the plated-wire output would not be wide enough to drive a logic circuit. The output of the blocking oscillator is connected to an input of the information flip-flop such that the output pulse will change the flip-flop from the reset, or 0, state to the set, or 1, state. The blocking oscillator is triggered by a negative signal from the read amplifier to provide the output pulse. A negative signal from the read amplifier is, therefore, defined as a binary 1. When a positive signal is applied to the blocking oscillator, no output pulse occurs, and the information flip-flop remains in the reset state.

The following are the functional requirements of the circuit:

Input—

Negative half sine wave, 100 nanoseconds in duration, 140 microamperes peak amplitude.

Output—

a. Greater than +3 volts in steady state

b. Capable of drawing 100 microamperes from a load at 0.5 volts for 0.5 microseconds.

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Repitition rate—

6.25 kilocycles

Power—

Less than 0.5 milliwatts

The amount of input signal required to trigger the blocking oscillator is specified in terms of current because the output of the read amplifier is a current source. The input signal has a duration of 100 nanoseconds because this time represents the minimum duration of the input signal. For an input of shorter duration, more triggering current would be required.

3.2.3.1. DESCRIPTION. The blocking oscillator is shown in Figure 32. The primary considerations in the design of the circuit are stability, triggering level, output pulse width, and power requirements. The blocking oscillator uses a transistor operated in the grounded-base configuration and a transformer to provide current gain such that when it is triggered, the loop gain is greater than one for the duration of the output pulse. Except when triggered, the loop gain of the circuit must be less than unity to maintain a stable circuit. The primary reason for using this configuration is that very low triggering levels are attainable with very low power requirements. The grounded-base operation of the transistor is more desirable than a common-emitter configuration because of its higher frequency response and lower input impedance for a given bias condition. The only limitation on the triggering because of the transformer is due to the winding capacitance.
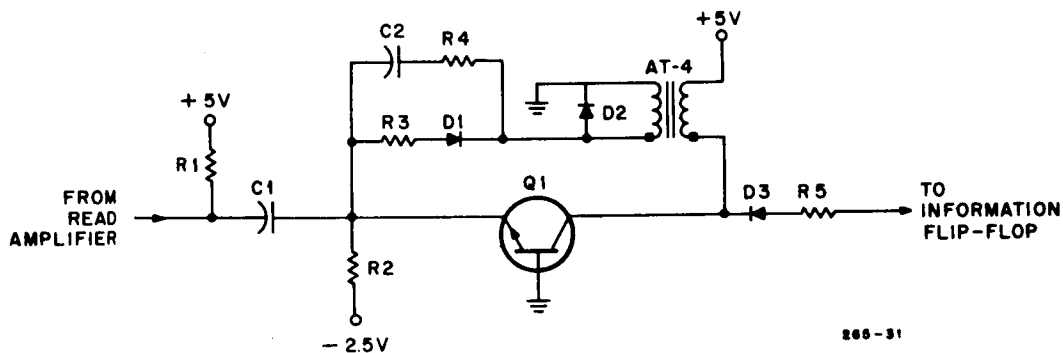
Figure 32.   Blocking Oscillator

The blocking oscillator basically goes through four separate states of operation. Starting from the quiescence the triggering state occurs when the input from the read amplifier is applied. After the circuit is triggered,

there is the turn-off state which determines the pulse width of the output. Following the turn-off state, there is the blocking, or recovery, state with the subsequent return to the quiescent state. Because of the importance of achieving low triggering levels, the triggering mechanism will be described first in order to show what limitations are imposed on the remaining design requirements.

When a 1 is being read out, a negative signal is applied to the blocking oscillator. This signal must trigger the blocking oscillator so that the output swings to ground to set the information flip-flop. Transistor Q1 is class-A biased in the quiescent state by means of the 2.5-volt supply providing emitter current through resistor R2. The collector of Q1 in the quiescent state is at the five-volt supply level. To trigger the blocking oscillator, the emitter current of Q1 must be increased by the triggering source so that the loop gain becomes greater than unity and the transistor will saturate. During this triggering time, diodes D1, D2, and D3 remain back-biased, and capacitors C1 and C2 provide voltage isolation and negligible impedance to the triggering currents. An a-c equivalent circuit of the blocking oscillator during the triggering is shown in Figure 33, where I_T is the triggering current source, C_s is the lumped transformer and transistor shunt capacitances, and h_{ib} is the transistor input impedance. Resistor R2
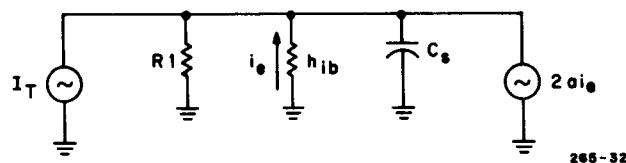
Figure 33. Equivalent Circuit of
Oscillator During Triggering

and the magnetizing inductance are large compared to the rest of the shunt paths and can be neglected. The equivalent current source $2\alpha_{ie}$ represents the change of collector current times the turns ratio of the transformer, which has a 2:1 current step-up ratio. The input impedance of the transistor, h_{ib}, is inversely proportional to the emitter current. This variation of h_{ib} allows the loop gain to be a function of the emitter current. In the quiescent state, h_{ib} is greater than R1, and more than half of any $2\alpha_{ie}$ current is shunted away from the emitter. When the emitter current, i_e, is increased by the triggering source, I_T, the loop gain is increased because

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the percentage of the $2\alpha_{ie}$ current shunted away from the emitter is de-
creased. The loop gain will become unity when the $2\alpha_{ie}$ current is equal to
the sum of the emitter current and the current shunted away from the emitter
by R1. The frequency response limitation of the circuit is due to the shunt
capacitance, C_s. The emitter voltage must be increased (becomes more nega-
tive) to increase the emitter current to the point at which the loop gain
reaches unity. Thus, C_s must be charged to the change of emitter voltage.
For a given waveshape of triggering current, I_T, an analysis is performed
to determine how much current is required in worst-case design to trigger
the blocking oscillator.

After the blocking oscillator is triggered, the feedback current in-
creases rapidly. Transistor Q1 saturates, and its collector voltage drops
below ground. Capacitor C2 is rapidly charged, and the feedback current
flows through the D1-R4 feedback loop. Diode D3 conducts when the collector
voltage goes below ground, and current is drawn through D3-R5 to set the in-
formation flip-flop. Capacitor C1 is also rapidly charged to the increased
emitter voltage and all of the feedback current flows into the emitter of
the transistor. During the initial portion of the pulse, the emitter cur-
rent will be 2α times the collector current, and, α being greater than 0.9,
the transistor is very heavily saturated. The emitter current will be con-
stant for the duration of the pulse, and the amount of the emitter current
is controlled by resistor R3 in the feedback loop. The collector current
increases linearly corrresponding to the linear increase of the magnetizing
current of the transformer. The transistor will remain saturated until the
collector current increases to α times the emitter current, at which time
the loop gain through the D1-R3 feedback loop becomes unity. When the tran-
sistor comes out of saturation, the collector voltage begins to go positive,
which, in turn, decreases the current through the feedback loop to the emit-
ter. This regenerative action causes the output pulse to end very rapidly.
The secondary of the transformer is clamped above ground by diode D2 for the
duration of the recovery of the transformer. Diodes D1 and D3 remain reverse
biased until the blocking oscillator is triggered by the next 1 in a read
cycle.

After the blocking oscillator pulse has ended, there are two conditions
that must be met during the recovery to the quiescent state. First, the cir-
cuit must not retrigger itself, and, second, the circuit must recover to the

quiescent state within 160 microseconds after the circuit is triggered because this amount of time represents the maximum duty cycle of the memory. When the pulse ends, the secondary of the transformer goes positive. This causes the emitter of the transistor to become reverse-biased because of the R4-C4 feedback loop. The R4-C2 and R1-C1 time constants are so small compared to the R2 (C1+C2) time constant that shortly after the pulse terminates, the amount of the emitter reverse bias is determined by the amount of the positive voltage swing of the secondary of the transformer, and capacitors C1 and C2 act as a voltage divider. The emitter voltage then begins to decay to its quiescent value because of the current being drawn through resistor R2 with a time constant of R2 (C1+C2). The magnetizing current of the transformer is recovered through diode D2. When the transformer is recovered, the voltage on the feedback loop goes from its clamped value to ground. This negative voltage change is transferred to the emitter through C1. The circuit is designed such that when the transformer recovers, the emitter voltage does not swing negative enough to retrigger the circuit. This is accomplished by reverse-biasing the emitter sufficiently to prevent the transistor from turning on when the transformer recovers. The pulse-to-pulse recovery requirement is met by making the R4 (C1+C2) time constant small enough to allow the transistor to return to quiescence by the time the next readout occurs.

The quiescent-state design condition is that the bias current of the transistor must be within certain limits as determined by the emitter current which is supplied from the 2.5-volt supply through resistor R2. The minimum emitter current determines the amount of triggering current required because at the lower emitter currents the amount which the emitter voltage must change to reach a loop gain of unity is increased so that the amount of charge which must be supplied to the shunt capacitance C_s (Figure 33) is also increased. The maximum emitter current is determined by the quiescent-state stability criterion. The small-signal a-c equivalent circuit used to analyze the quiescent-state stability is shown in Figure 34. Resistor R2 is large compared to h_{ib}, and resistor R4 is small as compared to the impedance of C2 at the frequencies of interest; they are not shown in the equivalent circuit. The impedance of capacitors C1 and C2 at the frequencies of interest are appreciable and are included. Capacitance C_s represents the lumped transformer and transistor capacitance; $2\alpha i_e$ represents the equivalent current source of the transformer feedback winding; L_s represents the primary

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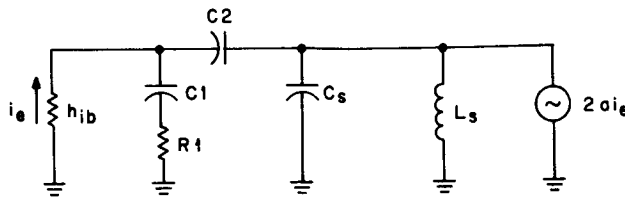
Figure 34. Small-Signal Equivalent
Circuit of Blocking Oscillator

magnetizing inductance transformed to the secondary; and h_{ib} represents the transistor input impedance. At a given frequency of $2\alpha i_e$ the circuit will become unstable when input impedance h_{ib} is lowered (corresponding to an increase in bias current) to the value at which the current source $2\alpha i_e$ can supply emitter current i_e to h_{ib} and to the circuit elements shunting h_{ib}. This instability occurs when the loop gain is equal to unity at the given frequency. The loop gain is frequency dependent, which can be seen intuitively from Figure 34. At very high frequencies, C_s will shunt most of the $2\alpha i_e$ current away from h_{ib}, and at very low frequencies, L_s will shunt most of the $2\alpha i_e$ current from h_{ib} with C2 acting as a high impedance. Therefore, the loop gain will be very low at the very high and very low frequencies. There is one frequency, defined as the resonant frequency, at which the loop gain is maximum. The nodal equations are solved at this frequency to determine the minimum allowable value of h_{ib} to have a loop gain less than unity in the quiescent state under worst-case conditions. From these equations, the maximum allowable bias of the transistor is determined, which, in turn, determines the minimum amount of triggering current required.

3.2.3.2. CIRCUIT DESIGN. The design equations of the blocking oscillator are solved in accordance with standard derating procedures unless otherwise noted. The following is a list of the values of the components used in the circuit of Figure 32.

Component	Value	Units
R1	1.00	K ohms
R2	124	K ohms
R3	200	ohms
R4	10.0	ohms
R5	2.61	K ohms
C1	1000	picofarads
C2	820	picofarads

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The transformer parameters used in the design equations are obtained from the AT-4 transformer specification. The transistor parameters used are obtained from the XT-173 specification, and the diode voltage drops are derived in conformance with the 1N-3207 specification.

The quiescent-state stability requirement is determined by solving for the resonant frequency of the circuit, and from this the minimum allowable input impedance is determined. It is then shown that the bias condition is such that the input impedance is never less than this minimum allowable value. The resonant frequency of the circuit is determined by equation (58), where ω_r is the resonant frequency, and the rest of the parameters are as defined in conjunction with Figure 34. The derivation of this equation is given under heading 3.2.4.3. of this report. In order to solve this equation under worst-case conditions, it must be determined at what temperature the

$$\omega_r^2 = \frac{C2(R1C1)^2 - C1L_s(C_s+C2) - L_sC2C_s}{(R1C1)^2L_sC2C_s} \tag{58}$$

worst-case stability requirement must be met. This will be explained in conjunction with Figure 35, which shows plots of the temperature variation of the maximum allowable emitter current to achieve quiescent-state stability and of the maximum bias of the transistor in the circuit. The maximum bias of the transistor increases with temperature because the variation of the base-emitter voltage variation of the transistor decreases with an increase of temperature. The variation of the maximum allowable emitter current is primarily due to the temperature variation of the input impedance, h_{ib}, and
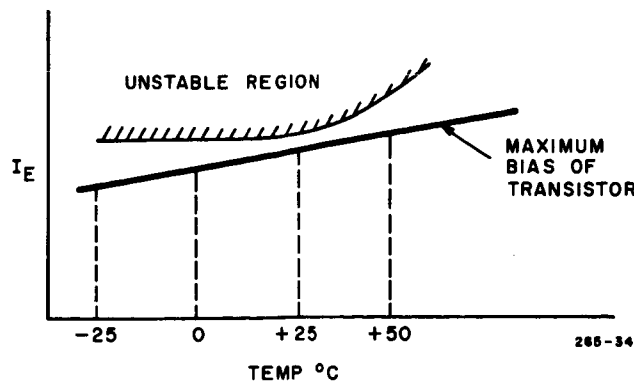
Figure 35. Bias Versus Frequency

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the transformer inductance, L_s. The input impedance is directly proportional to temperature, and the allowable bias current is, therefore, higher at the higher temperatures. The transformer core loss, which appears as a resistance shunting the $2\alpha i_e$ source shown in Figure 34, decreases with temperature and thus also makes the allowable bias current higher at the higher temperature. If it were not for the temperature variation of the transformer inductance, the worst-case stability condition would occur at the lowest temperature. The transformer inductance is practically constant for temperature above $25^\circ C$, but below this temperature it decreases rather rapidly. This decrease of inductance has the effect of increasing the resonant frequency, ω_r, as demonstrated by equation (58), which in turn shunts more of the $2\alpha i_e$ current through shunt capacitance C_s. Thus, the decrease of inductance has the effect of increasing the allowable bias current and cancels the effect of the variations of the transistor input impedance and of the transformer core loss. Below $25^\circ C$ there is practically no variation of allowable bias current with temperature, and the stability equations are solved at this temperature.

The worst-case value of ω_r is given by equation (59).

$$\omega_r^2 = \frac{\overline{C2}\,(\overline{R1}\underline{C1})^2 - \underline{C1}\overline{L_s}\,(\overline{C_s}+\overline{C2}) - \overline{L_s C2 C_s}}{(\overline{R1}\underline{C1})^2 \overline{L_s}\,C2\,C_s} \tag{59}$$

Substituting the values of the parameters into equation (59) and solving

$$\omega_r^2 = \frac{(900)(1.03\times900)^2\times10^{-30}-(900)(0.55)(55+900)\times10^{-27}-(0.55)(900)(55)\times10^{-23}}{(1.03\times900)^2(0.55)(900)(55)\times10^{-45}}$$

$$\tag{60}$$

$$\omega_r^2 = 11.4 \times 10^{12}$$

Thus, the worst-case oscillation frequency is 0.54 megacycles. The minimum allowable input impedance for quiescent-state stability is given by equation (61). The derivation of this equation is also given under heading 3.2.4.4.

$$h_{ib} = \frac{[1 + \omega_r^2 (R1C1)^2][1 + \omega_r^2 L_s (2\alpha C2 - C2 - C_s)]}{\omega_r^2 C1^2 R1 [\omega_r^2 L_s (C_s + C2) - 1]} \qquad (61)$$

The worst-case equation for determining the minimum allowable input impedance is given by equation (62).

$$\underline{h_{ib}} = \frac{[1 + \omega_r^2 (\overline{R1}\,\underline{C1})^2][1 + \omega_r^2 \overline{L_s} (\overline{2\alpha C2 - C2 - C})]}{\omega_r^2 \underline{C1}^2 \overline{R1} [\omega_r^2 \overline{L_s} (\overline{C_s + C2}) - 1]} \qquad (62)$$

Substituting the values of the parameters into equation (59) and solving

$$\underline{h_{ib}} = \frac{[1 + (11.9)(1.03)^2 (900)^2 \times 10^{-6}][1 + (11.9)(0.55)(2 \times 0.95 \times 900 - 900 - 55) \times 10^{-3}]}{10^{-9} \times (11.9)(900)^2 (1.03)[(11.9)(0.55)(900 + 55) \times 10^{-3} - 1]}$$

$$(63)$$

$$\underline{h_{ib}} = 1.32 \text{ kilohms}$$

This is the value of h_{ib} at which the loop gain will be equal to unity in the quiescent state under worst-case conditions. To achieve quiescent stability, the input impedance must be slightly greater than this value. The minimum h_{ib} as a function of emitter bias current at 25°C is given in equation (64). The input impedance has been derated five percent for life of the minimum value given on the transistor specification. Solving equations (63) and (64) gives a maximum allowable emitter bias current of

$$\underline{h_{ib}} = \frac{26.5}{I_E} 10^{-3} \text{ ohms} \qquad (64)$$

to have quiescent-state stability

$$\overline{I_E} = \frac{26.5 \cdot 10^{-3}}{1.32 \cdot 10^3} = 20.1 \text{ microamperes} \qquad (65)$$

The equation for determining the bias current of the transistor is

$$I_E = \frac{V_{EE} - V_{eb}}{R2} \qquad (66)$$

where V_{EE} is the 2.5-volt supply voltage and V_{eb} is the emitter-base voltage. The maximum emitter current is then

$$\overline{I_E} = \frac{\overline{V_{EE}} - V_{eb}}{\underline{R2}} = \frac{2.6 - 0.5}{120 \times 10^3} = 17.5 \text{ microamperes} \qquad (67)$$

The maximum emitter current is therefore less than the maximum allowable emitter current and the quiescent-state stability requirement has been met.

The minimum trigger current is determined at the maximum operating temperature, $50^\circ C$, because the input impedance is highest at the highest temperature. The higher input impedance means that the transistor must be turned on to a higher current in order to reach a loop gain of unity, and the worst-case conditions therefore occur at the higher temperature. The maximum input impedance has been derated five percent for life, and at $50^\circ C$ it is given by equation (68).

$$\overline{h_{ib}} = \frac{40.0}{I_E} 10^{-3} \text{ ohms} \qquad (68)$$

To determine the amount of triggering current required, it is necessary to determine first the value of emitter current required to make the loop gain unity. This will occur when the $2\alpha i_e$ current is large enough to supply the emitter current and the current to resistor R1. This is expressed by

$$2\alpha(I_{E2} - I_{E1}) = (I_{E2} - I_{E1}) + \frac{v_e}{R1} \qquad (69)$$

where I_{E2} and I_{E1} are the final and initial values of emitter current, respectively, and v_e is the change of the emitter voltage. Current I_{E2} occurs at the end of the triggering current. The change of emitter voltage is determined from the relationship

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$$\frac{dv_e}{d_{ie}} = h_{ib} \tag{70}$$

such that from equation (68)

$$v_e = 40.0 \times 10^{-3} \ln \frac{I_{e2}}{I_{e1}} \tag{71}$$

By combining equations (68), (69), and (71), the equation for determining the value of emitter current required to make the loop gain equal to unity at the end of the trigger current is

$$\frac{40.0 \times 10^{-3}}{\underline{R1}} \ln \frac{\overline{I_{E2}}}{\underline{I_{E1}}} = (\overline{I_{E2}} - I_{\underline{E1}})(2\underline{\alpha} - 1) \tag{72}$$

Current $I_{\underline{E1}}$ is simply the minimum quiescent state bias current at $50^{\circ}C$ and is

$$I_{\underline{E1}} = \frac{V_{EE} - \overline{V_{eb}}}{\overline{R2}} = \frac{2.4 - 0.64}{128 \times 10^3} = 13.9 \text{ microamperes} \tag{73}$$

substituting equation (73) into equation (72)

$$\frac{40.0 \times 10^{-3}}{970} \ln \frac{\overline{I_{E2}}}{13.9 \times 10^{-6}} = (\overline{I_{E2}} - 13.0 \times 10^{-6})(2 \times 0.92 - 1) \tag{74}$$

Solving equation (74) for $\overline{I_{E2}}$

$$\overline{I_{E2}} = 124 \text{ microamperes} \tag{75}$$

By substituting equation (73) and (75) into equation (71), the change of emitter voltage required to give a loop gain of unity is found to be

$$v_{e2} = 40.0 \ln \frac{124}{13.9} = 87.5 \text{ millivolts} \tag{76}$$

To determine the amount of triggering current required for a given waveshape of triggering current the nodal equation for the circuit of Figure 33 must be solved. It is desirable to solve this equation for a triggering current whose waveshape is a half sine wave since this approximates the waveshape of the output of the read amplifier. The change of emitter current, i_e, as a function of a change of emitter voltage is determined from the relationship of equation (71)

$$i_e = I_{E1}(e^{25v}-1) \tag{77}$$

The nodal equation for the equivalent circuit of Figure 33 can then be written as

$$I_T \sin\frac{\pi}{T}t = \frac{V_e}{R1} + C_s\frac{dV_e}{dt} - (2a-1)I_{E1}(e^{25v}e-1) \tag{78}$$

where T is the switching time of the triggering current and I_T is the peak value of the half sine wave. Because of the last term in equation (78) an exact solution is impossible by using elementary techniques. A very close approximate solution can be obtained rather easily however. It is known that at time t = 0, $dV_e/dE = 0$ due to the presence of the shunt capacitance. It is also known that at time t = T the desired solution has $dV_e/dt = 0$, since this means that a loop gain of unity has been reached at the end of the triggering current. The final value of the emitter voltage, v_e, has already been determined by equation (76), and the initial value of v_e is obviously zero. The approximate solution to equation (78) of the form given in equation (79) is suggested. The three terms on the right side of equation (78) are tabulated in Table 4 using T = 100 nanoseconds, which

$$v_e = \frac{v_{e2}}{2}(1-\cos\frac{\pi}{T}t) \tag{79}$$

corresponds to the minimum switching time of the output of the amplifier. The input required to solve equation (79) is also tabulated and plotted

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in Figure 36, from which it can be seen that the tabulated input corresponds very closely to a perfect sine wave.
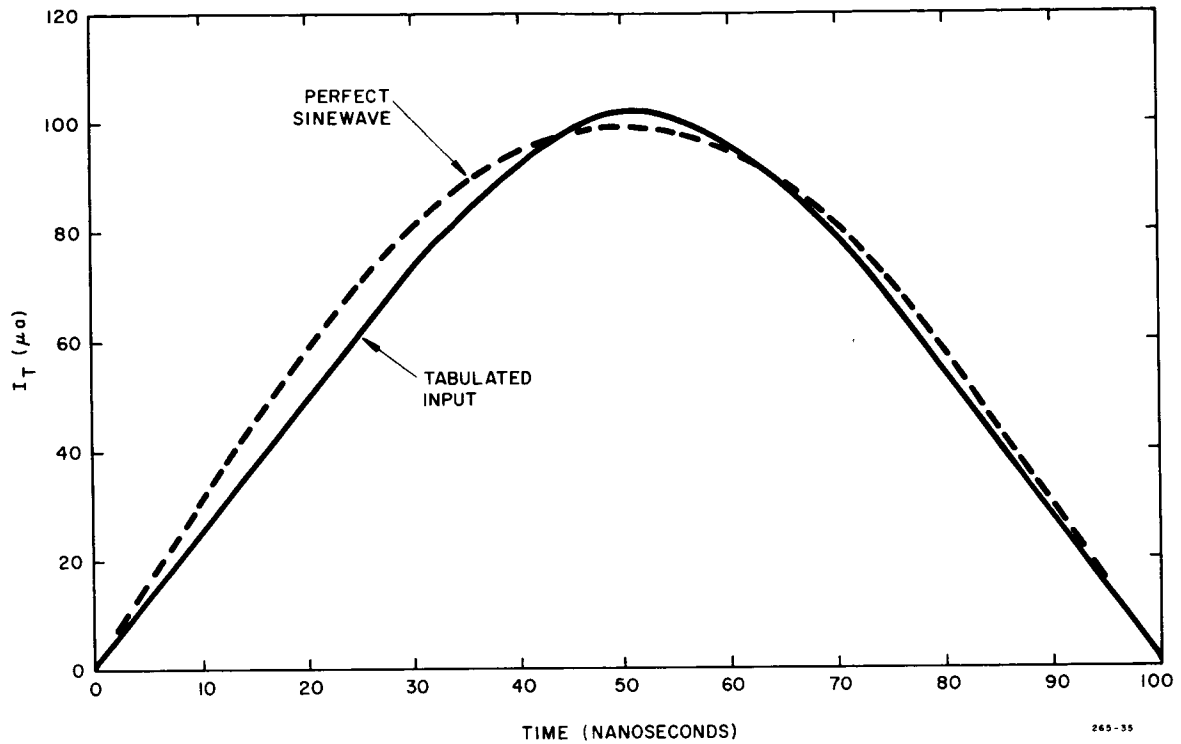
Figure 36. Input Signals to Blocking Oscillator

Table 4. Tabulation of Triggering Current

t	v_e (mv)	$\dfrac{v_e}{970}$ (µa)	$550^{-12} \dfrac{dv_e}{dt}$ (µa)	$(20.92-1)(13.9)(3^{25v}-1)$ (µa)	I_T
0	0.00	0.00	0.00	0.0	0.0
10	2.15	2.21	23.3	0.7	24.8
20	8.40	8.96	44.3	2.5	50.7
30	18.1	18.6	61.0	6.4	73.2
40	30.3	31.2	72.0	12.6	90.6
50	43.8	49.0	75.6	22.1	102.5
60	57.5	58.9	72.0	36.0	94.9
70	69.7	71.5	61.0	52.8	79.7
80	79.2	81.5	44.3	70.0	55.8
90	85.4	87.8	23.3	83.7	27.4
100	87.5	90.0	0.0	90.0	0.0

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The peak value of the triggering current required for a loop gain of unity is 103 microamperes. Generally, a 20-percent overdrive must be supplied for a stable trigger. The minimum trigger current required is therefore

$$\underline{I_T} = 1.2 \ (103) \ \text{microamperes} = 124 \ \text{microamperes} \tag{80}$$

which is less than required by the circuit specification.

The blocking oscillator must supply a pulse which has a minimum duration of 0.5 microseconds, and it must draw a minimum current of 100 microamperes at 0.5 volts from the information flip-flop. When the blocking oscillator is triggered, the collector voltage goes from 5 volts to below ground, as expressed by equation (81). The amount of current which flows through the R3-D1 feedback loop is the emitter current of the transistor during the pulse and is expressed by equation (82).

$$v_c = V_{cc} + V_{eb} - V_{ce} \tag{81}$$

$$i_e = \frac{\frac{v_c}{2} - V_{D1} - V_{eb}}{R3} \tag{82}$$

where V_{eb} and V_{ce} are the emitter-base and collector-emitter drops of the transistor, and V_{D1} is the drop of diode D1. The collector current increases from its initial value because of the magnetizing inductance of transformer L_M.

$$i_c = \frac{i_e}{2} + \frac{v_c}{L_M} t \tag{83}$$

The pulse width is terminated when the transistor begins to recover from saturation. If this recovery occurs at time T, equation (83) becomes

$$i_e \, (a-0.5) = \frac{v_c}{L_M} \, T \qquad\qquad (84)$$

By substituting equations (81) and (82) into (84) and solving for T, the equation which determines the pulse width is obtained as follows.

$$T = \frac{L_M \, (a-0.5)}{R3} \, (0.5 - \frac{V_{d1} + V_{eb}}{V_{CC} + V_{eb} - V_{ce}}) \qquad\qquad (85)$$

The minimum worst-case pulse width will occur at -20°C because of the increased diode drops and the decreased magnetizing inductance. The worst-case equation is

$$\underline{T} = \frac{\underline{L_M} \, (a-0.5)}{\overline{R3}} \, (0.5 - \frac{\overline{V_{d1}} + \overline{V_{eb}}}{\underline{V_{CC}} + \overline{V_{eb}} - \overline{V_{ce}}}) \qquad\qquad (86)$$

Substituting worst-case values

$$\underline{T} = \frac{1.6 \times 10^{-3} \, (0.89 - 0.5)}{206} \, (0.5 - \frac{0.87 + 0.99}{4.8 + 0.99 - 0.26}) \qquad\qquad (87)$$

or $\quad \underline{T} = 0.5$ microseconds as desired.

The maximum pulse width is useful to know because this figure is used to calculate the worst-case power requirements. The worst-case equation for the maximum pulse width is

$$\overline{T} = \frac{\overline{L_M} \, (\overline{a} - 0.5)}{\underline{R1}} \, (0.5 - \frac{V_{d1} + V_{eb}}{\underline{V_{CC}} + V_{eb} - V_{ce}}) \qquad\qquad (88)$$

The pulse width is practically constant for temperature variations above 25°C. The maximum pulse width can therefore be determined as occurring at 25°C.

$$\overline{T} = \frac{2.3 \times 10^{-3}(0.99-0.5)}{194} \quad (0.5 - \frac{0.67 + 0.70}{5.2 + 0.70 - 0.14}) \tag{89}$$

$$\overline{T} = 1.72 \text{ microseconds}$$

Because of the large bit transients that occur during a write cycle, it is possible for sufficient current to sneak through the output transistor of the read amplifier to trigger the blocking oscillator. If this sneak current occurs, the information in the information flip-flop must not be changed during the time the bit current is present because the information being written would change. The method used to ensure that the flip-flop does not change state is described in this report under heading 3.2.4. It is sufficient at this point to state that it is necessary to limit the output current of the blocking oscillator. This is accomplished by means of resistor R5 in series with logic diode D3. Diode D3 is located in the blocking oscillator module to provide isolation of the capacitance of the connection between the blocking oscillator and the information flip-flop when the blocking oscillator is triggered. The output current of the blocking oscillator when the load is at 0.5 volts is

$$I_o = \frac{0.5 + V_{eb} - V_{ce} - V_{D3}}{R5} \tag{90}$$

where V_{D3} is the drop across diode D3. The minimum worst-case output current, I_o, is determined at room temperature because the temperature coefficients of V_{eb} and V_{D3} cancel each other.

$$I_o = \frac{0.5 + V_{eb} - \overline{V_{ce}} - \overline{V_{D3}}}{\overline{R5}} \tag{91}$$

Substituting the worst-case values

$$\underline{I_o} = \frac{0.5 + 0.56 - 0.2 - 0.59}{2.68 \times 10^3} = 101 \text{ microamperes} \tag{92}$$

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which is sufficient to set the information flip-flop. It is necessary to know the maximum output current of the blocking oscillator when the bit current is present. The maximum load voltage during this time is 2.25 volts. The worst-case equation is therefore

$$\overline{I}_o = \frac{2.25 + \overline{V_{eb}} - \underline{V_{ce}} - \underline{V_{D3}}}{\underline{R5}} \tag{93}$$

Substituting and solving:

$$\overline{I}_o = \frac{2.25 + 0.97 - 0.14 - 0.40}{2.53 \times 10^3} = 1.05 \text{ milliamperes} \tag{94}$$

After the pulse has terminated, the emitter is reverse-biased because the positive voltage swing on the secondary of the transformer is coupled through capacitor C2. When the transformer recovers, the negative voltage swing on the secondary of the transformer, which is equal to the voltage drop of diode D2, must not retrigger the blocking oscillator. By the time the transformer recovers, the reverse bias on the emitter is determined only by capacitors C1 and C2, which act as a voltage divider for the positive voltage swing that occurred when the pulse terminated. When the transformer recovers, the full negative voltage swing of diode D2 is transferred to the emitter because resistor R1 is much larger than resistor R4. The voltage at the emitter at the instant the transformer recovers is

$$V_{er} = \frac{C2}{C1 + C2} \left(\frac{V_{CC} + V_{eb1} - V_{ce}}{2} + V_{D2} \right) - V_{eb1} - V_{D2} \tag{95}$$

where V_{eb1} is the emitter-base voltage and V_{ce} the collector-emitter voltage during the pulse, and V_{D2} is the voltage drop of diode D2 during the transformer recovery. The R2 (C1+C2) time constant is very long in comparison with the time required for the transformer to recover; thus, the decay of the emitter voltage caused by this time constant can be neglected for purposes of calculating v_{er} (see Figure 37). The circuit is designed so that v_{er} is less than the amount of emitter voltage at which the transistor will conduct any significant current. Expressed in worst-case terms

99
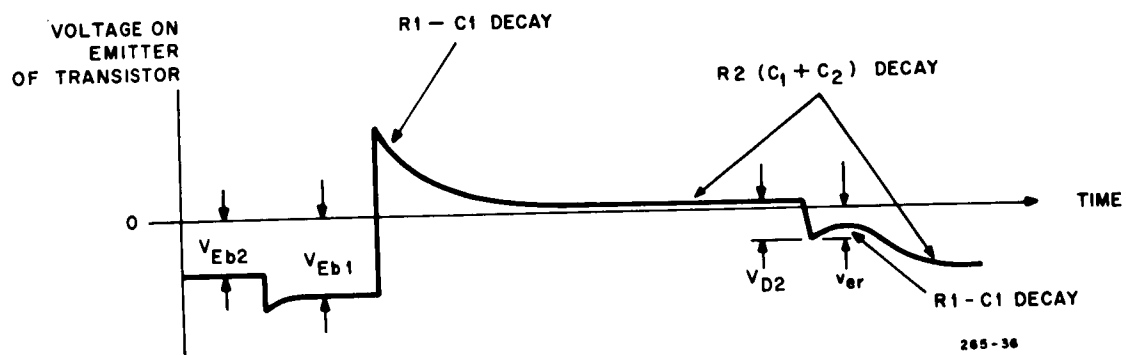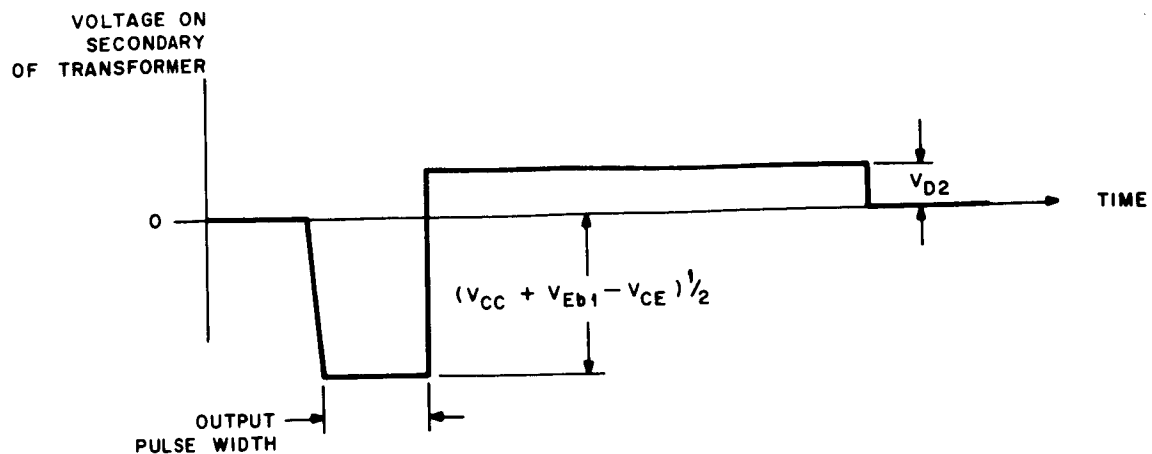
Figure 37.   Switching Waveshapes of Blocking Oscillator

$$\overline{v}_{er} = \frac{C2}{\overline{C1} + \underline{C2}} \left(\frac{V_{CC} + \overline{V_{ebl}} - \overline{V_{ce}}}{2} + \overline{V_{d2}} \right) - \overline{V_{ebl}} - \overline{V_{D2}} \tag{96}$$

This equation is solved at the lowest operating temperature because the diode drops are largest at that temperature.   Substituting the worst-case values and solving

$$= \frac{740 \times 10^{-12}}{(1100 + 740)10^{-12}} \left(\frac{4.9 + 0.92 - 0.26}{2} + 1.0 \right) - 0.92 - 1.0$$

$$= -0.4 \text{ volts}$$

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Since $\overline{V}_{er}$ is less than the voltage at which the transistor will begin to conduct, the circuit cannot retrigger itself and become free running.

To achieve pulse-to-pulse recovery, the emitter voltage must recover to the quiescent state emitter voltage, V_{e2}. Equation (98) describes the

$$(V_{EE} - V_{eb1} + \frac{V_{CC} + V_{eb1} - V_{ce}}{2} \frac{C2}{C1 + C2}) \, e^{-T/R2(C1+C2)} = V_{EE} - V_{eb2} \quad (98)$$

recovery time, T, in reference to the 2.5-volt supply voltage, V_{EE}, since the emitter voltage decays towards this value until the quiescent value is reached. Solving for T

$$T = -R2 \, (C1+C2) \, n \, \frac{V_{EE} - V_{eb2}}{V_{EE} - V_{eb1} + \frac{V_{CC} + V_{eb1} - V_{ce}}{2} \frac{C2}{C1 + C2}} \quad (99)$$

The worst-case recovery time is

$$\overline{T} = -\overline{R2} \, (\overline{C1+C2}) \, n \, \frac{V_{EE} - \overline{V_{eb2}}}{\underline{V_{EE}} - \overline{V_{eb1}} + \frac{(\overline{V_{CC}} + \overline{V_{eb1}} - V_{ce}) \, \overline{C2}}{2(\overline{C1+C2})}} \quad (100)$$

Substituting and solving $\qquad\qquad\qquad\qquad\qquad\qquad (101)$

$$\overline{T} = - \, (128 \times 10^3)(1100+900)10^{-12} \, \ln \frac{2.4 - 0.73}{2.4 - 0.92 + \frac{(5.1+0.92-0.14)900 \times 10^{-12}}{2(1100+900)10^{-12}}}$$

or

$$\overline{T} = 142 \text{ microseconds}$$

Since $\overline{T}$ is less than 160 microseconds, the pulse-to-pulse recovery requirement is met.

3.2.3.3. POWER SUPPLY REQUIREMENTS. The amount of power required for the operation of the circuit is found by determining the steady-state power and by averaging the transient power over the maximum duty cycle. The steady-state power is determined by the transistor biasing. It is assumed for the purposes of the power determination that the transistor α is unity, and the

$$P_{SS} = I_E \ (V_{EE} + V_{CC}) \qquad (102)$$

collector supply voltage V_{CC} must supply all the emitter current. In worst-case calculations the steady-state power is

$$P_{SS} = \overline{I_E} \ (\overline{V_{EE} + V_{CC}}) \qquad (103)$$

where $\overline{I_E}$ is given by equation (67). The worst-case steady-state power is therefore

$$P_{SS} = 17.5 \times 10^{-6} \ (2.6 + 5.1) = 0.13 \ \text{milliwatts}$$

The transient power occurs during the output pulse of the blocking oscillator. This power is supplied from the collector supply V_{CC} and is determined by the collector current as expressed in equation (83). If the transistor α is made equal to unity for worst-case power analysis, equation (83) can be rewritten as follows

$$i_e = \frac{i_e}{2} \ (1 + \frac{t}{T}) \qquad (104)$$

where T is the pulse width of the output. The average collector current during the pulse is

$$i_{e-av} = \frac{3}{4} \ i_e \qquad (105)$$

where i_e is expressed by equation (82). Equation (105) then becomes

$$i_{c-av} = \frac{3}{4} \frac{(V_{CC}+V_{eb}-V_{ce})/2 - V_{d1} - V_{eb}}{R3} \qquad (106)$$

In worst-case calculations

$$\overline{i_{c-av}} = \frac{3}{4} \frac{(\overline{V_{CC}}+\underline{V_{eb}}-\underline{V_{ce}})/2 - \underline{V_{d1}} - \underline{V_{eb}}}{\underline{R3}} \qquad (107)$$

Substituting and solving

$$\overline{i_{c-av}} = \frac{3}{4} \frac{(5.1+0.70-0.14)/(2-0.67-0.70)}{194} = 5.63 \text{ milliamperes} \qquad (108)$$

The average transient power in worst-case calculations is

$$\overline{P_{T-av}} = \frac{\overline{V_{CC}} \; \overline{i_{c-av}} \; \overline{T}}{\underline{T_R}} \qquad (109)$$

where T_R is the minimum time between cycles (160 microseconds), and $\overline{T}$ is 1.72 microseconds as given by equation (89). The worst-case transient power is therefore

$$= \frac{(5.1)(5.63-10^{-3})(1.72\times10^{-6})}{160 \times 10^{-6}} \qquad (110)$$

or

$$\overline{P_{T-av}} = 0.31 \text{ milliwatts}$$

Therefore, the total power requirement of the circuit is the sum of the transient and steady-state power, or 0.44 milliwatts. In addition to this power, the leakage current of the bypass capacitor on the 5-volt supply must be included. For a derated leakage current of ten microamperes this adds

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0.05 milliwatts to the above figure for a total power requirement of 0.49 milliwatts.

Because of the high sensitivity of the blocking oscillator, the following filtering is provided in each blocking oscillator on the 5-volt supply (Figure 38).
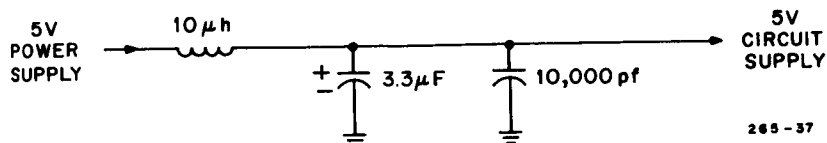
Figure 38. Filtering of Blocking Oscillator

Two bypass capacitors are used to provide good filtering at high frequencies through the small capacitor, which has a much lower inductance than the 3.3-microfarad capacitor; the 3.3-microfarad capacitor provides good filtering at the lower frequencies.

3.2.3.4. DERIVATION OF EQUATIONS. The derivations of equations (58) and (61), which are used to meet the stability requirements of the blocking oscillator, are set forth under this heading. Figure 34 shows the equivalent circuit used to derive these equations. The nodal equations for this circuit are

$$0 = e_1 \left(\frac{1}{h_{ib}} + \frac{j\omega C1}{1 + j\omega C1R1} + j\omega C2\right) - e_2 \ (j\omega C2) \qquad (111)$$

$$2\alpha i_e = -e_1 \ (j\omega C2) + e_2 \left(\frac{1}{j\omega L_s} + j\omega C + j\omega C2\right) \qquad (112)$$

These equations are written as a general function of frequency. The resonant frequency ω_r can be determined from them, and the value of h_{ib} at which the circuit becomes unstable can be found.

$$e_2 = \frac{e_1}{j\omega C2} \left(\frac{1}{h_{ib}} + \frac{j\omega C1}{1 + j\omega C1R1} + j\omega C2\right) \qquad (113)$$

Substituting equation (113) into equation (112)

(114)

$$2\alpha i_e = e_1 [-j\omega C2 + \frac{1}{j\omega C2}(\frac{1}{h_{ib}} + \frac{j\omega C1}{1 + j\omega C1R1} + \omega C2)(\frac{1}{j\omega L_s} + j\omega C_s + j\omega C2)]$$

Rearranging the terms of equation (114)

$$2\alpha i_e + \frac{e_1}{h_{ib}}(\frac{1}{\omega^2 C2 L_s} - \frac{C_s + C2}{C2}) =$$

(115)

$$je_1 [-\omega C2 + (\frac{\omega C1}{1 + j\omega C1R1} + \omega C2)(- \frac{1}{\omega^2 C2 L_s} + \frac{C_s + C2}{C2}$$

Instability occurs when the $2\alpha i_e$ source is large enough to supply i_e current to h_{ib}, or, in equation form

$$e_1 = i_e h_{ib} \tag{116}$$

Substituting equation (116) into equation (115) and rearranging

$$i_e [2\alpha + \frac{1 - \omega^2 L_s(C_s + C2)}{\omega^2 C2 L_s}] =$$

(117)

$$-j i_e h_{ib}[\omega C2 + \frac{\omega C1 + \omega C2 + j\omega^2 C1 C2 R1}{1 + j\omega C1R1} \cdot \frac{1 - \omega^2 L_s(C_s + C2)}{\omega^2 C2 L_s}]$$

By multiplying numerator and denominator of the last term in equation (117) by $1 - j\omega C1R1$ equation (118) is obtained.

$$2a + \frac{1 - \omega^2 L_s (C_s + C2)}{\omega^2 C2 L_s} =$$

$$-jh_{ib}\left[\omega C2 + \frac{[C1 + C2 + (\omega C1R1)^2 C2 - j\omega C1^2 R1][1 - \omega^2 L_s(C_s + C2)]}{[1 + (\omega C1R1)^2]\omega L_s C2}\right. \tag{118}$$

Equation (118) shows that the imaginary terms on the right side must equal zero, which therefore divides equation (118) into two separate equations, (119) and (120). In terms of the circuit, this means that current i_e is in phase with current source $2ai_e$.

$$2a + \frac{1 - \omega^2 L_s(C_s + C2)}{\omega^2 C2 L_s} = -h_{ib}\frac{\omega C1^2 R1[1 - \omega^2 L_s(C_s + C2)]}{[1 + (\omega C1R1)^2]\omega L_s C2} \tag{119}$$

$$0 = \omega C2 + \frac{[C1 + C2 + (\omega C1R1)^2 C2]\cdot[1 - \omega^2 L_s(C_s + C2)]}{[1 + (\omega C1R1)^2\omega L_s C2} \tag{120}$$

Equation (119) can now be solved by h_{ib} as a function of the circuit parameters and frequency ω.

$$h_{ib} = \frac{[1 + \omega^2(R1C1)^2][1 + \omega^2 L_s(2aC2 - C2 - C_s)]}{\omega^2 C1^2 R1[\omega^2 L_s(C_s + C2) - 1]} \tag{121}$$

This is equation (61), which is used to determine the maximum allowable bias of the blocking oscillator transistor. The value of ω^2 to be used in the solution of equation (121) is determined by the auxiliary equation which relates ω to the circuit parameters. From equation (120)

$$\omega^4 - \omega^2\frac{C2(R1C1)^2 - C1L_s(C_s + C2) - L_s C2 C_s}{(R1C1)^2 L_s C2 C_s} - \frac{C1 + C2}{(R1C1)^2 L_s C2 C_s} = 0 \tag{122}$$

There are two values of ω^2 which satisfy the equation (122), one of which is over 100 times larger than the other. These two values of ω^2 are the values at which the derivative of the loop gain with respect to ω is equal to zero, or, in other words, the maxima of the loop gain versus frequency curve. The loop gain is an absolute maximum at the higher value of ω, which is therefore defined as the resonant frequency ω_r. In solving for ω_r, the last term of equation (122) can be neglected.

$$\omega_r^2 = \frac{C2(R1C1)^2 - Ci1_s(C_s+C2) - L_sC2C_s}{(R1C1)^2 L_s C2 C_s} \tag{123}$$

Equation (123) is identical to equation (58).

3.2.4. BIT DRIVER

Specifications

When information is to be written into the memory during a write operation, a current is passed down the plated wire. The waveshapes of the write currents are shown in Figure 39. The timing of the bipolar waveshapes is accomplished by the two bit clocks. The function of the bit driver is to drive the bit current down the plated wire. If a binary 1 is stored in the information flip-flop, the 1-bit current will be driven, and if a binary 0 is stored in the information flip-flop, the 0-bit current will be driven. Therefore, the bit driver must drive one of two current waveshapes, depending upon the state of the information flip-flop, whose amplitude is within the defined limits. Accordingly, the following specification is written for the bit driver:

Inputs—

    a. Two timing pulses sequentially applied at ground in the inactive state and at 11.46 to 12.14 volts in the active state

    b. Logic outputs of the information flip-flop

Output Current—

    a. Bipolar waveshape

        binary 1—positive followed by negative
        binary 0—negative followed by positive
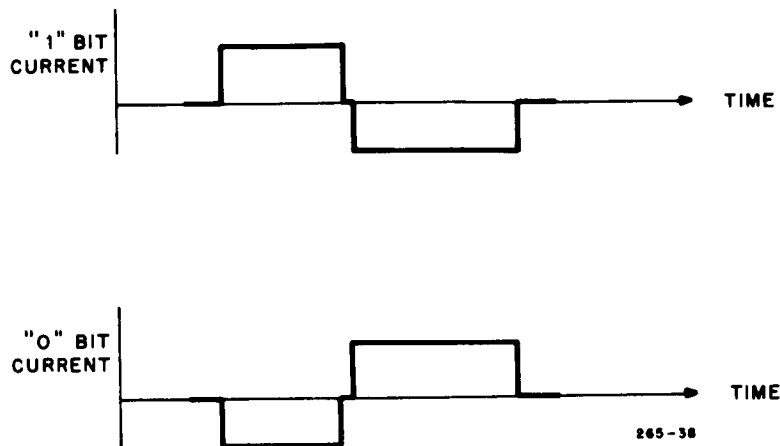
Figure 39. Waveshapes of
Write Currents

b. Amplitude

Positive current—35 milliamperes ±5 percent
Negative current—35 milliamperes ±5 percent

The tolerance on bit current for changes during the life of
the memory is ±5 percent. There is an additional tolerance
of ±11 percent due to initial tolerances on all the components
in the drive circuits. The operating point was selected to
maximize operating margins and only the change with aging is
significant with respect to the operating margins given in
Section 5.

c. Rise Time

50 nanoseconds (maximum)

Maximum Average Power—

0.65 milliwatts

3.2.4.1. DESCRIPTION. The circuitry involved in the design of the bit
driver is shown in Figure 40. Resistor R_L represents the resistance of a

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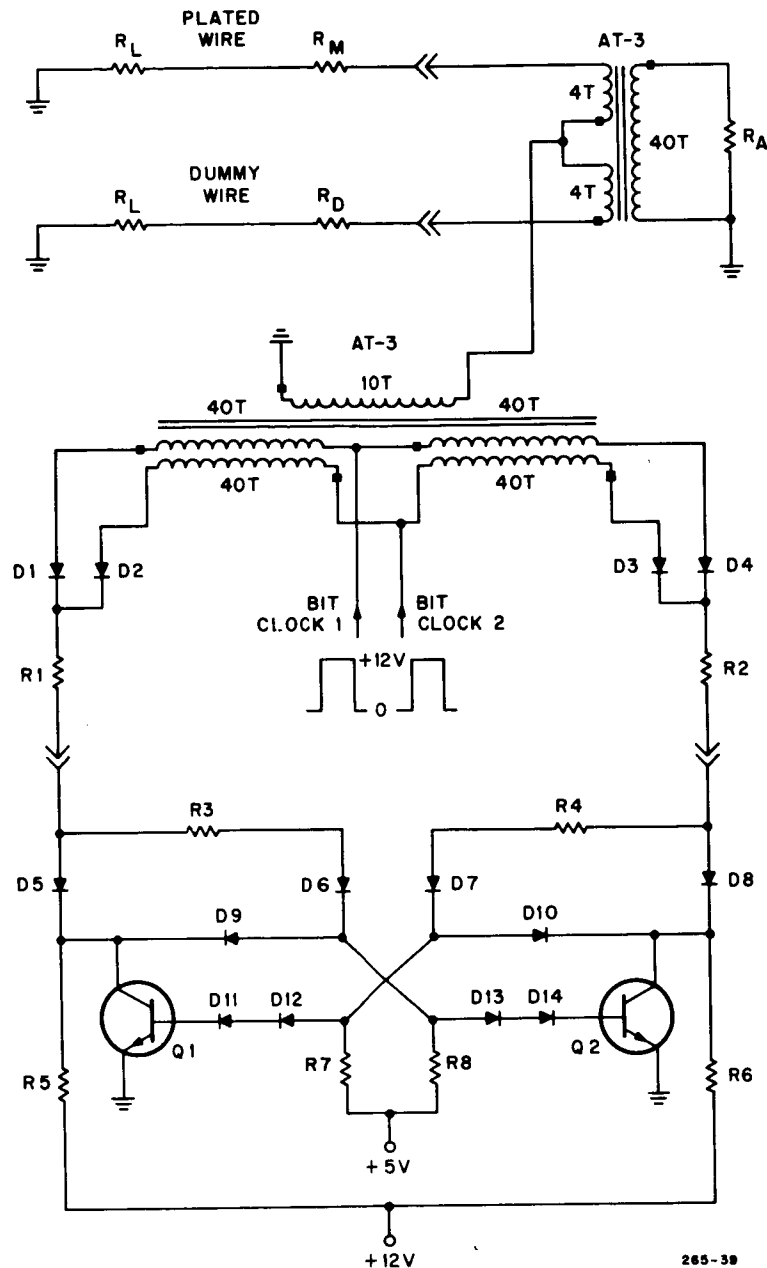
Figure 40. Schematic Diagram of
Bit-Driver Circuitry

plated wire and of the dummy wire. Resistor R_M represents the resistance
of the bit-sense matrix, and R_D is a resistor which provides some cancella-
tion of the bit transient to reduce the loading effect of the read amplifier
on the bit current. Resistor R_A is the input impedance of the first stage
of the read amplifier. The AT-3 transformer consists of windings on two
separate torroids as indicated by the separation in Figure 40. The AT-3
transformer, diodes D1 through D4, and resistors R1 and R2 are packaged in

the read amplifier module. The rest of the components are packaged in the information register module. Transistors Q1 and Q2, diodes D9 through D14, and resistors R7 and R8 are components forming the information flip-flop. Only that portion of the information flip-flop necessary to the understanding of the operation of the bit driver is shown so that the logic inputs and outputs to the flip-flop are not shown in Figure 40. When one of the transistors in the flip-flop is conducting, the other is nonconducting. When the bit clocks are not present, diodes D5 through D8 are reverse-biased, thereby providing isolation between the flip-flop and the connections between the information register module and the read amplifier module. Because of the symmetry of the circuit, the method by which the bit current is derived can be explained with reference to only one of the bit clocks and by showing only the half of the flip-flop which is conducting current. Assuming that transistor Q1 is conducting before the bit clock is applied, Figure 41 shows only the portion of the circuitry which will be conducting current before or during the application of bit clock 1. Diodes D1 through D4 provide winding isolation so that the windings to which a bit clock is applied are not short-circuited by the windings to which the other bit clock is applied. The loading of the read amplifier is small and will be ignored for the present. The only effect of this loading is to increase the percentage of variation of the bit currents.

Referring now to Figure 41, prior to the application of the bit clock in a write cycle, diodes D5 and D7 are reverse-biased. Transistor Q1 is saturated with the base current supplied through resistor R7 and the collector current supplied through R8. Whether or not Q1 is conducting is determined by the information to be written into the memory because during a write cycle, the information flip-flop is used to store the information until it is written into the memory by the bit current. If Q1 is conducting, a 1 is to be written. When the bit clock is applied, current I_1 flows through diode D1 to the collector of Q1. Transistor Q1 must remain saturated when I_1 flows into the collector, but the base current from resistor R7 by itself is too low to maintain this condition. For this reason, additional base current (I_2) is supplied from the bit clock through diode D4. Therefore, the current level of the flip-flop is increased by the bit clock so that the bit current can be derived without amplification of the flip-flop current. The bit current I_4 is one half of the I_3 current, ignoring the loading effects of the read amplifier, which, in turn, is four times the difference between the
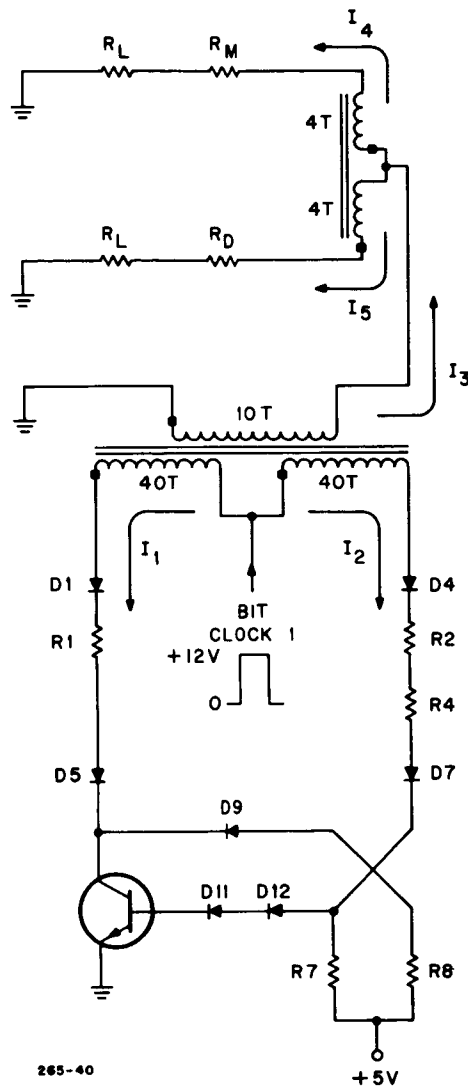
Figure 41. Partial Schematic
Diagram of Bit-Driver Circuitry

I_1 and I_2 currents. Resistors R1 and R2, which have the same resistance, and resistor R4 are chosen to have the desired value of bit current. Current I_2 is made large enough to keep Q1 in saturation in worst-case conditions. When the current level of the flip-flop is increased by the bit clock, the nonconducting transistor must remain nonconducting. This is assured because the voltage at the anode of diode D5, which is only the sum of the diode drop and the collector-emitter saturation voltage of Q1, is insufficient to overcome the diode drops of D6, D13, D14, and the base-emitter drop of Q2; thus, the base current to the nonconducting transistor is negligible.

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Bit clock 2 is applied immediately after bit clock 1 is terminated, and the operation of the circuit is identical to that described above except that the I_1 and I_2 currents flow through the windings to which bit clock 2 is applied. Since these windings have the polarity markings reversed from the windings to which bit clock 1 was applied, the polarity of the bit current is reversed. Therefore, when transistor Q1 is conducting, the bit current is a bipolar waveshape comprised of a positive current followed by a negative current which writes a 1 as desired. If the flip-flop is in the reset, or 0 state, transistor Q2 is conducting, and the I_1 and I_2 currents flow to its collector and base, respectively. Therefore, the application of the bit clocks causes a bipolar bit current whose polarities are reversed from the condition in which the flip-flop is in the 1 state, and a 0 is written.

Resistors R5 and R6 are used to maintain the collector of the off transistor at 12 volts so that the diode in series with the collector remains reverse-biased when the bit clock is applied. This isolates the capacitance of the off transistor from the active portion of the circuitry, thereby improving the rise time of the bit current. The primary limitation on the rise time is the method by which the transformer is wound. If the windings are very closely coupled, the rise time is fast because of the low leakage inductance between the windings to which the bit clocks are applied and the ten-turn secondary winding, but an overshoot will occur if the capacitance between the windings is too high. Accordingly, the transformer is wound such that the capacitance does not cause bit current overshoots, and the rise time is limited by the leakage inductance to approximately 50 nanoseconds.

3.2.4.2. CIRCUIT DESIGN. The design of the bit driver requires that resistors R1 through R4 be determined to achieve the desired bit current and to assure that the on transistor in the information flip-flop remains saturated. The following is the component list for the bit driver:

R1	412 ohms
R2	412 ohms
R3, R4	1.87 K ohms
D1—D10	1N3207
D11—D14	MC-456
Q1, Q2	XT-169

Standard derating is used in the design unless otherwise noted. The determination of the bit current and its tolerance is done primarily by determining currents I_1 and I_2 (Figure 41). This is done by determining the diode drops in the current path and by applying Ohms law. Equations (124) through (126) give the nominal and worst-case values of currents I_1 and I_2. These equations ignore temperature effects and the loading effect of the read amplifier, both of which can be considered separately to determine the bit-current tolerance. The diode drops have only been derated ten percent for life in determining the current tolerance. This is felt to be justified since the probability that they would all go to their worst-case values is very small.

$$I_1 = \frac{8.92}{R1} = \frac{8.92}{412} = 21.7 \text{ milliamperes} \tag{124}$$

$$\overline{I_1} = \frac{9.94}{R1} = \frac{9.94}{412} = 24.1 \text{ milliamperes} \tag{125}$$

$$\underline{I_1} = \frac{7.90}{R1} = \frac{7.90}{412} = 19.2 \text{ milliamperes} \tag{126}$$

$$I_2 = \frac{9.50}{R2 + R4} = \frac{9.50}{2282} = 4.2 \text{ milliamperes} \tag{127}$$

$$\overline{I_2} = \frac{10.10}{R2 + R4} = \frac{10.10}{2282} = 4.4 \text{ milliamperes} \tag{128}$$

$$\underline{I_2} = \frac{8.90}{R2 + R4} = \frac{8.90}{2282} = 3.9 \text{ milliamperes} \tag{129}$$

The bit currents are therefore

$$I_{bit} = 2(I_1 - I_2) = 2(21.7 - 4.2) \text{ milliamperes} = 35 \text{ milliamperes} \tag{130}$$

$$\overline{I_{bit}} = 2(\overline{I_1} - \underline{I_2}) = 2(24.1 - 3.9) \text{ milliamperes} = 40.4 \text{ milliamperes} \tag{131}$$

$$\underline{I_{bit}} = 2(\underline{I_1} - \overline{I}) = 2(19.2 - 4.4) \text{ milliamperes} = 29.6 \text{ milliamperes} \tag{132}$$

The actual variation of the bit current is somewhat less than calculated in equations (131) and (132) since the variation of the stabilization effects of the diode resistances and the load resistance have been ignored for ease of calculation. The loading effect of the amplifier will occur if there is an unbalance between the resistances in the plated-wire path and the dummy-wire path. Note that the matrix resistance, R_M, is the resistance of the matrix transistors to the large bit currents and is lower than the small signal resistance it presents to the plated-wire signal. Resistance R_M is determined from the V_{CE} specification on the matrix transistors. Resistor R_D is chosen to be approximately the same as the minimum R_M so that the plated-wire signal loss is kept small. Therefore, the loading effect of the amplifier will only affect the minimum bit current tolerance which occurs when R_M is maximum. Furthermore, the loading will only occur on the negative bit current. The read amplifier impedance is only low when a positive voltage appears on the 40-turn winding because this turns the input impedance of the first transistor stage in the amplifier to a low impedance. Resistance R_A then becomes approximately 1000 ohms (resistor R2 of Figure 30). The minimum negative bit current then becomes

$$\underline{-I_{bit}} = \underline{2I_{bit}}\ \frac{\underline{R_A} + 50(\underline{R_D} + R_L)}{2\underline{R_A} + 50(2R_L + \underline{R_D} + \overline{R_M})} \tag{133}$$

Substituting and solving

$$\underline{-I_{bit}} = 2 \times 29.6\ \frac{1000 + 50(3.8 + 4.5)}{2000 + 50(9.0 + 3.8 + 8.0)}\ \text{milliamperes} \tag{134}$$

$$= 27.8\ \text{milliamperes}$$

The variation of the bit current with temperature is very small and can be ignored. The variation of the bit current with temperature is caused by the change of the voltage drops across the diodes in the I_1 and I_2 current paths (Figure 41). Current I_1 increases with an increase of temperature because of the negative temperature coefficient (T.C.) of diodes D1 and D5, but I_2, which is subtracted from I_1 when determining the bit current, also increases because of the temperature coefficient of diodes D4, D7, D11, D12,

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and the base-emitter diode of transistor Q1. Assuming all of the diodes have a T.C. of 1.8 millivolts/°C, the change of bit current for a 40°C change of temperature is

$$\Delta I_{bit} = \frac{2 \ (T.C.) \ \Delta T}{R1} - \frac{5 \ (T.C.) \ \Delta T}{R2 + R4}$$

$$= \frac{2(1.8 \times 10^{-3}) \ 40}{412} - \frac{5(1.8 \times 10^{-3}) \ 40}{2282} \qquad (135)$$

$$= 0.21 \ \text{milliamperes}$$

The actual variation is less than this because the T.C. of the MC-456 diodes is higher than that of the 1N3207 diodes. The bit currents can therefore be expressed as

$$+I_{bit} = 35, \ \pm 5.6 \ \text{milliamperes}$$

$$-I_{bit} = 35, \ +5.6, \ -7.2 \ \text{milliamperes}$$

or, in terms of percentage

$+I_{bit}$ = 35 milliamperes, ±16 percent which is ±5 percent for aging and ±11 percent for initial tolerance.

$-I_{bit}$ = 35 milliamperes, +16 percent, -20 percent which is ±5 percent for aging and +11 percent, -15 percent for initial tolerance.

As mentioned under the description of the read amplifier, it is possible for the blocking oscillator to be triggered because of the bit transient sneaking through the last stage of the read amplifier. If the information flip-flop is in the reset state, a 0 is being written, but if the blocking oscillator is triggered, the output current of the blocking oscillator turns off the conducting transistor. To avoid this possibility, the I_2 current is made large enough to supply both the base current of the conducting transistor and the output current, I_o, of the blocking oscillator. The minimum base current to the conducting transistor is

$$I_b = I_2 - \overline{I_0} \qquad (136)$$

where I_0 is given in equation (94), and I_2 is given in equation (129).
Substituting and solving

$$I_b = 3.9 \text{ milliamperes} - 1.05 \text{ milliamperes} = 2.85 \text{ milliamperes} \qquad (137)$$

The maximum collector current I_c is I_1 of equation (125). Therefore, the maximum circuit beta is

$$\overline{B_{cct}} = \frac{\overline{I_c}}{I_b} = \frac{24.1}{2.85} = 8.5 \qquad (138)$$

To keep the conducting transistor in saturation the maximum circuit beta must be less than the minimum transistor beta, which is 12; this requirement is met as shown by equation (138). The output current of the blocking oscillator could set the flip-flop after the bit current terminates, but since the flip-flops are always reset before the next memory cycle, the change of state becomes irrelevant.

The circuit requires no steady-state power since all the power is supplied by the bit clocks. The average power of the bit driver is simply

$$\overline{P} = \overline{E_s}(\overline{I_1 + I_2}) \frac{\overline{T_1} + \overline{T_2}}{T_R} \qquad (139)$$

where E_s is the 12-volt supply voltage, T_R is the time between write cycles, and T_1 and T_2 are the pulse widths of bit clocks 1 and 2, respectively.
Substituting and solving

$$\overline{P} = 12.24 \ (24.1 + 4.4) \ \frac{(0.1 + 0.2) \times 10^{-6}}{160 \times 10^{-6}} \times 10^{-3} = 0.65 \text{ milliwatts} \qquad (140)$$

3.3. WORD SELECTION AND COUNTER CIRCUITS

The memory counters have been designed for a low-power aerospace memory operating with a maximum counting rate of 160 microseconds (memory bit rate of ten microseconds). The information under this heading is concerned with the design of the A-counter and driver, B-counter and driver, P-counter and driver, A amplifier, and line current regulators.

3.3.1. DESCRIPTION OF OPERATION

3.3.1.1. WORD SELECTION CIRCUITS. The word lines are selected by means of the configuration shown in Figure 42. Each word line contains 12 words taking advantage of the nondestructive readout property of the plated wire to
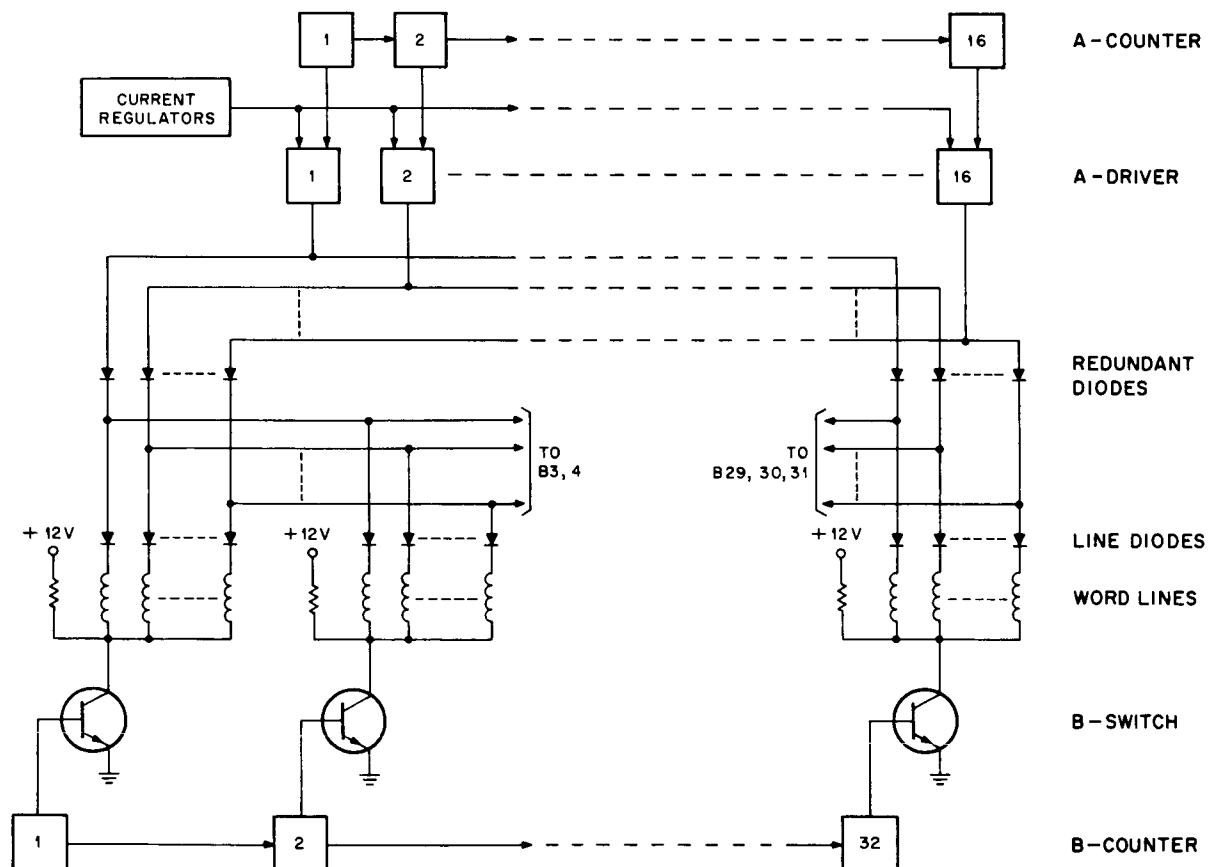
Figure 42. Word-Line Selection Matrix

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reduce power consumption and minimize component count. Selection of a word line is done by means of a diode matrix. The matrix includes a redundant diode for every four diodes to prevent a complete loss of the memory if one of the line diodes should become shorted. It can be shown that by using this redundant diode a failure of one of the line diodes allows a maximum of 4/512 of the memory to become inoperable. These diodes are also used to decrease the effective capacitance on the A driver end of the word line. The memory has 32 B switches and 16 A drivers, which allow one of 512 word lines to be selected. A ring counter was used to cycle and drive each set of edge drivers and switches. The standby power for the A and B ring counters is 12 milliwatts total.

3.3.1.2. B-COUNTER SWITCH. Figure 43 shows the B-counter-switch circuit. The individual stages of the counter are made up of complementary pairs of transistors connected in a regenerative configuration. The counter is cleared by pulsing the clear and set inputs. When cleared, the first stage is turned on, and the remaining stages in the counter are turned off. The counter is thus placed at a count of 1 in the standby state. In the standby state the anode and gate currents (I_{65}, I_1) are 250 microamperes. Current I_{65} is the hold current for the counter, and I_1 is used to propagate the 1 count through the ring. Note that in the standby state driver transistor Q69 is off. Transistor Q69 is turned on when a power pulse is applied to Q66. Transistor Q66 conducts and provides a current of 150 milliamperes used to put transistors Q1 and Q2 in a hard loop (increase current level at which the regeneration is occurring). The turning on of Q69 causes its associated group of word lines to be brought to ground potential. The power pulse has a duration of 500 nanoseconds. After the power pulse ends, the counter portion of the circuit is stepped by a pulse applied to Q65. Transistor Q65 conducts and diverts the holding current I_{65} to ground. Transistors Q1 and Q2 are turned off, and a positive pulse is coupled to the NPN transistor of the succeeding stage. When the step pulse ends, the anode line is returned to a positive potential by I_{65}. The stage which is turned on by the positive pulse from the previous stage is held on by holding current I_{65}. Stage 2 is illustrated in Figure 43; since it operates basically the same way that the other 31 stages operate it is not necessary to discuss this stage.
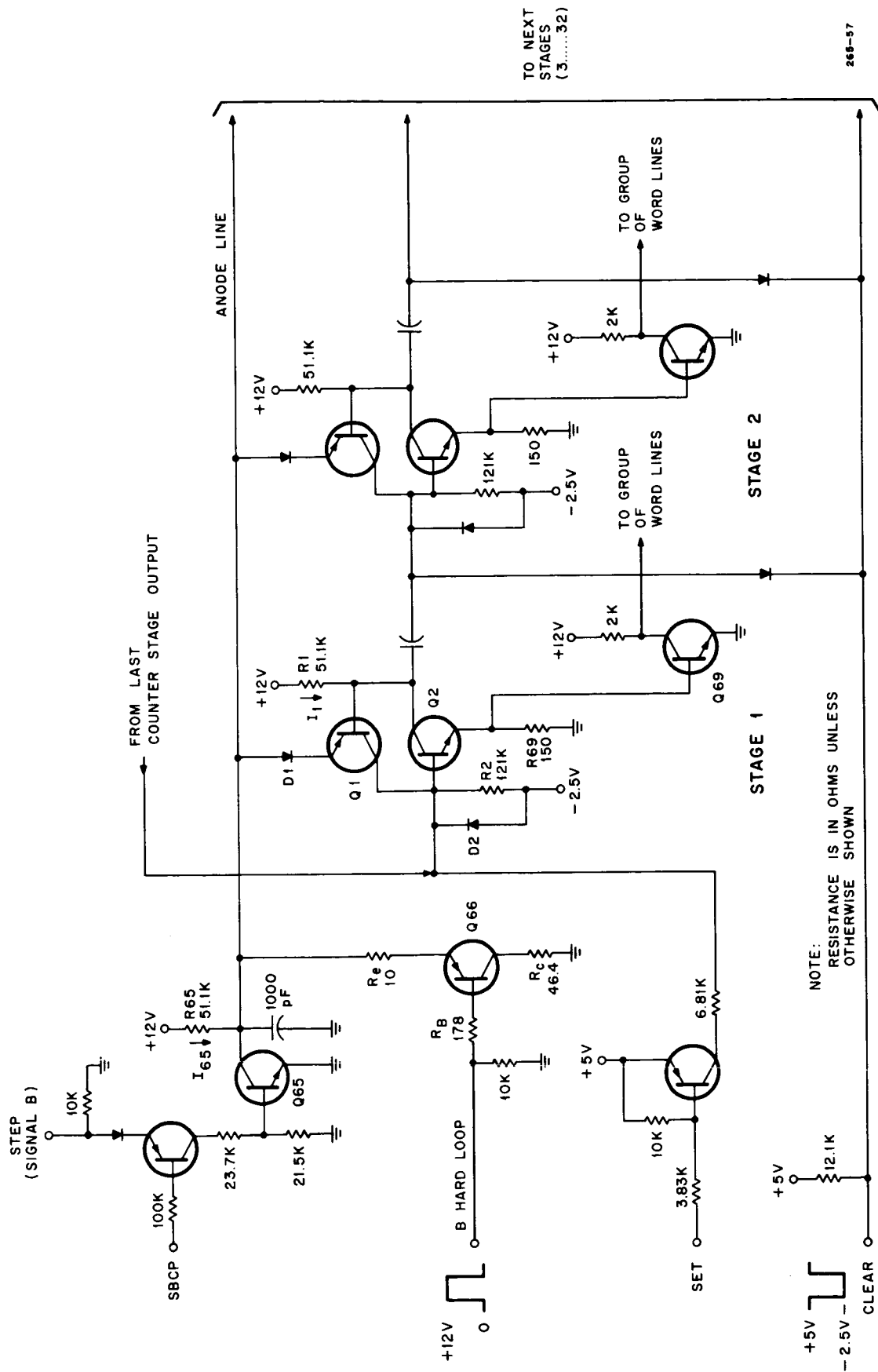
Figure 43.   B-Counter and Driver

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3.3.1.3. A-COUNTER AND DRIVER. The counter portion of the A-counter and driver (Figure 44) is identical to that of the B-counter and driver except that the driver portion uses two transistors (Q3 and Q4 in stage 1) instead of one. The circuit operation is also similar in that a power pulse is applied to the circuit to establish a high-current loop in the selected stage. Assuming that stage 1 is selected, the stage receives a power pulse via Q66, and while this pulse is present a current pulse is applied to the emitter line via the base regulator circuit. This pulse turns on Q3 and Q4 allowing current to flow down the word strap. The word current pulse has a duration of approximately 150 nanoseconds and a rise time of 35 nanoseconds. Unselected stages are reverse – biased by +12 volts from the counter circuit to prevent any possible sneak currents from flowing.

3.3.1.4. P-COUNTER AND DRIVER. The means of selecting a word within a word line is performed by the P-counter and driver (see Figure 45). This counter is a 12-stage counter and selects a group of 16 bit-sense matrix circuits out of 192 circuits. The P-counter portion of the circuit is identical to the A-counter and B-counter described previously. The driver outputs of this counter driver are positive and negative 6-volt signals that supply current to the bases of the matrix transistors. The push-pull output is developed by means of a bipolar wound transformer.

3.3.1.5. MISCELLANEOUS WORD SELECTION CIRCUITS. The remaining circuits that are required in the counters are the set and clear circuits. These circuits, as the name implies, are used to clear the A-counter, B-counter, and P-counter to the first address. These circuits are typical and should require no explanation.

The final circuits required for word selection are the regulators. These circuits are used to regulate the word current. They are connected into the system, as shown in Figure 42. Appreciable power has been saved in these circuits since they are pulsed on and off.

3.3.2. SPECIFICATIONS FOR CIRCUITS AND COMPONENTS

Under this heading are presented the specifications for the various circuits and components.

Figure 44. A-Counter and Driver

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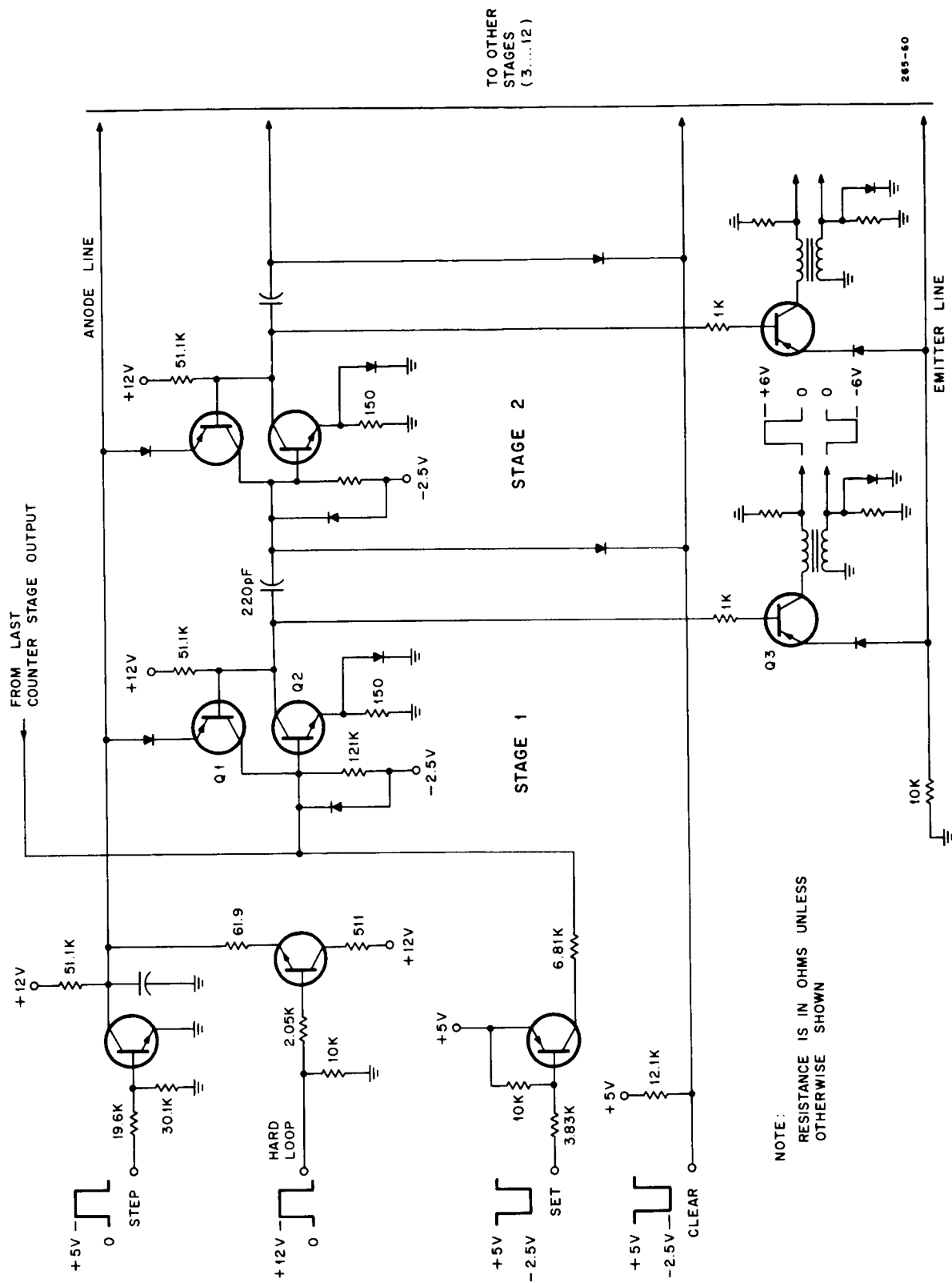
Figure 45. P-Counter and Driver

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3.3.2.1. COUNTER CIRCUITS.

Signal	Circuit		
	B-Counter	A-Counter	P-Counter
Input step pulse			
Pulse width	1µs	1µs	1µs
Current	0.5 ma	0.5 ma	0.5 ma
Voltage	+5V	+5V	+5V
Polarity	Positive	Positive	Positive
Hard pulse			
Pulse width	—	280 ns	2.1µs
Current	—	5 ma	5 ma
Voltage	—	12V	12V
Polarity	—	Positive	Positive
Drive pulse			
Pulse width	280 ns	150 ns	2.1µs
Current	40 ma	180 ma	60 ma
Voltage	12V	24V	12V
Polarity	Positive	Positive	Positive
Clear pulse			
Pulse width	25µs	25µs	25µs
Current	5 ma	5 ma	5 ma
Voltage	5V	5V	5V
Polarity	Positive	Positive	Positive

3.3.2.2. TRANSVERSE CURRENT CIRCUIT.

Amplitude:	860 milliamperes
Rise time:	35 nanoseconds ±5 nanoseconds
Pulse width:	150 nanoseconds
Rate:	160 microseconds

3.3.2.3. COMPONENTS.

Power Supplies

+12, +5, -2.5 volts	±1% supply regulation
	±1% d-c distribution
	±2% transients

Semiconductors

Line Driver:	2N2477 (selected)
Counter (PNP):	2N2828 (selected)
Counter (NPN):	2N2501 (selected)
Line Diodes:	1N3207 (selected)
Logic Diode:	1N3207 (selected)
Redundant Diode:	FDS 622 (selected)

Maximum diode drops and transistor saturation voltages as given in the specifications are derated in accordance with the Aerospace Memory Component Derating Report (Technical Report No. 238-1 Rev. A 8/1/63) except where noted.

3.3.3. DESIGN EQUATIONS

The steady-state equations will be expressed showing the calculations used to check the operation of the circuit. These calculations are not to determine the optimum operation of the circuits but rather to check the values chosen using worst-case values. In many cases the requirements of the circuits can be met so easily that worst-case values will be chosen that could not possibly exist. Such assumptions make the circuit more reliable and simplify the amount of calculations necessary by an order of magnitude.

3.3.3.1. B-COUNTER AND DRIVER. To understand the operation of the circuit, refer to Figure 46. In the standby configuration (a), the amount of current in the emitter of the PNP is equal to the current in R1. Assuming the current in each branch is two units and divides as shown, the beta required by the circuit is 3. Other combinations of current division will also allow
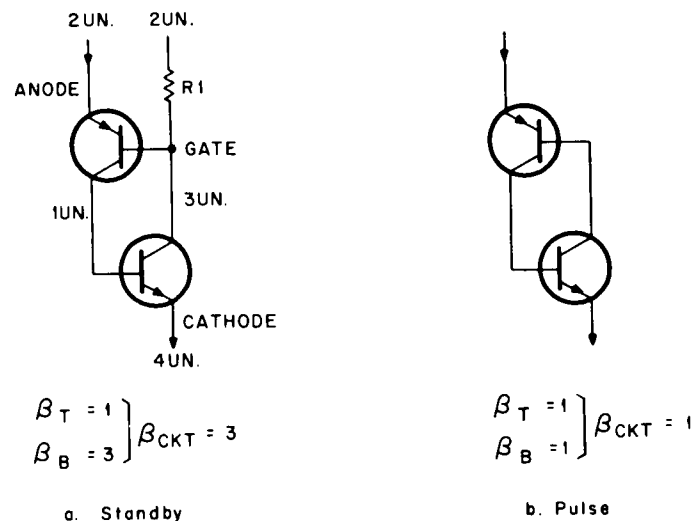
Figure 46. Basic Counter Configuration

the circuit to operate with both lower and higher circuit betas. Since this is a minimum beta condition required for proper operation, the other combination need not be discussed. Figure 46 (b) shows an equivalent circuit for

the drive pulse condition. Since the drive current is much higher than the standby current the current in the **R** branch is negligible and therefore can be neglected. Here it is found that all that is necessary for proper operation is to have $\beta_{CKT} > 1$. Both transistors have been specified as follows:

25°C, NPN and PNP

$$h_{FE} = 10 \qquad I_c = 200 \text{ microamperes} \qquad V_{CE} < 0.3$$

$$h_{FE} = 10 \qquad I_c = 150 \text{ milliamperes} \qquad V_{CE} < 0.4$$

If now we derate the transistor for variations due to temperature and life:

$$h_{FE_{EOL}} = h_{FE} \times \text{effect of life} \times \text{effect of temperature}$$

$$= 10 \times 0.6 \times 0.66 = 3.9$$

The above straightforward equations show that the minimum beta requirements are met for both the 200-microampere and 150-milliampere levels.

All requirements on breakdown voltages for the transistors and diodes have been derated by a minimum of 2 (see Table 5).

Table 5. Breakdown Voltages

	NPN		PNP	
	Actual	Spec.	Actual	Spec.
V_{CE}	12	25	3.5	25
V_{BE}	2.5	6	Diode protected	4
V_{BC}	14.5	30	14.5	30

The B-counter and driver is shown in Figure 43. We can now proceed to check the choice of component values that have been specified for the circuit.

Standby Condition. The first item that we can check is the maximum forward bias on the B line driver in its standby state, and the worst-case circuit beta for the standby condition.

$$\overline{i_H} = \frac{\overline{V_S} - V_{Ce_2}}{\underline{R1} + \underline{R69}} + \frac{\overline{V_S} - (V_D + V_{Be} + V_{Ce_2})}{\underline{R65} + \underline{R69}}$$

Since R65 = R1 and assume drops are zero.

$$\overline{i_H} = \frac{2(\overline{V_S})}{\underline{R65} + \underline{R69}} = \frac{2(1.04)(12)}{0.97(51.1K + 150\Omega)}$$

$$\overline{i_H} = 504 \text{ microamperes.}$$

$$\overline{V_{Be_{69}}} = (504 \times 10^{-6})(150 \times 1.03) = 78 \text{ millivolts}$$

$$\underline{i_A} = \frac{V_S - (\overline{V_D} + \overline{V_{Be_2}} + \overline{V_{Ce_1}})}{\overline{R65} + \overline{R64}}$$

$$\overline{V_D} = 1.2(0.6) + 2.5(50) = 0.72 + 0.125 = 0.9$$

$$\overline{V_{Be_2}} = 1.2(0.8) + 2.5(50) = 0.96 + 0.125 = 1.1$$

$$\overline{V_{Ce_1}} = 1.3(0.3) = 0.39 = 0.4$$

$$\underline{i_A} = \frac{0.97(12) - (0.9 + 1.1 + 0.4)}{1.03(51.1^k + 0.15^k)} \quad \frac{11.5 - 2.4}{52.8}$$

$$\underline{i_A} = 172 \text{ microamperes}$$

If we assume that the current divides as shown in Figure 47a then the circuit beta would be:

$$\beta_{CKT} \frac{402}{100} \times \frac{100}{72} = 5.6$$

Using the end-of-life values for the transistors as 3.9, the circuit beta would be 15.2(3.9×3.9). This shows that the circuit requirement is much less than the available beta.
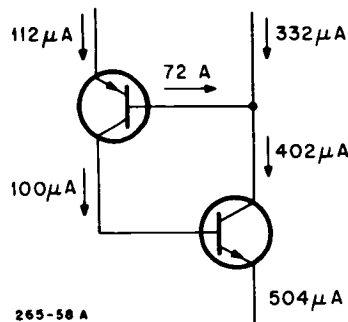
Figure 47a. Basic B-Counter Configuration

<u>Drive Condition</u>. It is possible also to calculate the operation of the circuit during the drive state. These calculations are as follows:

$$\overline{V_S} = 1.04(12) = 12.5 \text{ volts}$$

$$\underline{V_S} = 0.96(12) = 11.5 \text{ volts}$$

$$i_{e_{66}} = i_{b_{66}} + i_{c_{66}}$$

$$i_{b_{69}} = i_{c_{66}} - \frac{V_{Be}}{R69}$$

$$\overline{V_A} = \overline{V_D} + \overline{V_{Ce_1}} + \overline{V_{Be_2}} + \overline{V_{BC_{69}}}$$

$$\overline{V_{Ce_1}} = 1.3(0.3) = 0.39$$

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$$\overline{V_{Be_2}} = 1.2(1.35) + 2.5(50) = 1.62 + 0.125 = 1.745$$

$$\overline{V_{Be_{69}}} = 1.2(1.5) + 2.5(50) = 1.8 + 0.125 = 1.925$$

$$\overline{V_A} = 1.4 + 0.39 + 1.745 + 1.925 = 5.46 \text{ volts}$$

$$\underline{V_A} = \underline{V_D} + \underline{V_{Ce}} + \underline{V_{Be_2}} + \underline{V_{Be_{69}}}$$

$$\underline{V_D} = 0.8(0.9) - 2.5(75) = 0.72 - 0.1875 = 0.532$$

$$\underline{V_{Ce_1}} = 0.9(0.1) = 0.090$$

$$\underline{V_{Be_2}} = 0.8(1.2) - 2.5(75) = 0.96 - 0.1875 = 0.772$$

$$V_{Be_{69}} = 0.8(1.2) - 2.5(75) = 0.96 - 0.1875 = \underline{0.772}$$

$$\underline{V_A} = 2.166 \text{ volts} \qquad\qquad 2.166$$

$$V_S = V_{ce_{66}} + V_A + I_e R_c + I_c R_c$$

$$= V_{ce} + V_A + I_e R_e + I_e R_c - I_B R_c$$

$$V_S = V_{ce_{66}} + V_A + I_e(R_e + R_c) - I_B R_c$$

$$V_S = V_{Be_{66}} + V_A + I_e R_e + I_B R_B$$

$$I_{B_{66}} = \frac{V_S - V_{Be_{66}} - V_A - I_c R_e}{R_B}$$

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$$V_S = V_{ce_{66}} + V_A + I_e(R_e + R_c) - \frac{R_c}{R_B}[V_S - V_{Be_{66}} - V_A - I_e R_e]$$

$$V_S = V_{ce_{66}} + V_A + I_e(R_e + R_c) - \frac{R_c}{R_B}V_S + \frac{R_c}{R_B}(V_{Be_{66}} + V_A) + \frac{R_c}{R_B}I_e R_e$$

$$V_S - V_{ce_{66}} - V_A + \frac{R_c}{R_B}V_S - \frac{R_c}{R_B}(V_{Be_{66}} + V_A) = I_e(R_e + R_c) + I_e(\frac{R_c}{R_B}R_e)$$

$$V_S - V_{ce_{66}} - V_A + \frac{R_c}{R_B}(V_S - V_{Be_{66}} - V_A) = I_e(R_e + R_c + \frac{R_c}{R_B}R_e)$$

$$I_{e_{66}} = \frac{V_S - V_{ce_{66}} - V_A + \frac{R_c}{R_B}(V_S - V_{Be_{66}} - V_A)}{R_e + R_c + \frac{R_c}{R_B}R_e}$$

$$\overline{I_{e_{66}}} = \frac{\overline{V_S} - \underline{V_{ce}} - \underline{V_A} + \frac{R_c}{R_B}(\overline{V_S} - \underline{V_{Be}} - \underline{V_A})}{\underline{R_e} + \underline{R_c} + \frac{R_c}{R_B}\underline{R_e}}$$

$$\overline{I_{e_{66}}} = \frac{12.5 - 0.18 - 2.16 + \frac{46.4}{178}(12.5 - 1.1 - 2.16)}{0.97(10 + 46.4 + \frac{46.4}{178} \times 10)}$$

$$\overline{I_{e_{66}}} = 220 \text{ milliamperes}$$

$$\underline{I_{e_{66}}} = \frac{\underline{V_S} - \overline{V_{ce}} - \overline{V_A} + \frac{\overline{R_c}}{R_B}(\underline{V_S} - \overline{V_{Be}} - \overline{V_A})}{\overline{R_e} + \overline{R_c} + \frac{\overline{R_c}}{R_B}(\overline{R_e})}$$

$$I_{e_{66}} = \frac{11.5 - 0.5 - 5.46 + \frac{46.4}{178}(11.5 - 1.5 - 5.46)}{1.03(10 + 46.4 + \frac{46.4}{178} \times 10)}$$

$$I_{e_{66}} = 110 \text{ milliamperes}$$

$$V_S = V_{ce} + V_A + I_e(R_e + R_c) - I_B R_c$$

$$V_S = V_{Be} + V_A + I_e R_e + I_B R_B$$

$$I_{e_{66}} = \frac{V_S - V_{Be} - V_A - I_B R_B}{R_e}$$

$$V_S = V_{ce} + V_A + (R_e + R_c)\left\{\frac{V_S - V_{Be} - V_A - I_B R_B}{R_e}\right\} - I_B R_c$$

$$V_S = V_{ce} + V_A + (\frac{R_e + R_c}{R_e})(V_S - V_{Be} - V_A) - \frac{R_e + R_c}{R_e}(I_B R_B) - I_B R_c$$

$$V_S = V_{ce} + V_A + (\frac{R_e + R_c}{R_e})(V_S - V_{Be} - V_A) - I_B\left\{\frac{R_B(R_e + R_c)}{R_e} + R_c\right\}$$

$$I_{B_{66}} = \frac{V_{ce} + V_A + (\frac{R_e + R_c}{R_e})(V_S - V_{Be} - V_A) - V_S}{\frac{R_B(R_e + R_c)}{R_e} + R_c}$$

Minimum and Maximum Load on Input

$$\overline{I_{B_{66}}} = \frac{\underline{V_{ce}} + \underline{V_A} + (\frac{\overline{R_e + R_c}}{\underline{R_e}})(\overline{V_S} - \underline{V_{Be}} - \underline{V_A}) - \overline{V_S}}{\frac{R_B(R_e + R_c)}{\underline{R_e}} + \underline{R_c}}$$

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$$\overline{I_{B_{66}}} = \frac{0.8 + 2.16 + (\frac{10+46.4}{10})(12.5-1.1-2.16) - 12.5}{0.97\frac{178(46.4+10)}{10} + 46.4}$$

$$\overline{I_{B_{66}}} = 41.7 \text{ milliamperes}$$

$$\underline{I_{B_{66}}} = \frac{\overline{V_{ce}} + \overline{V_A} + (\frac{\overline{R_e}+\overline{R_c}}{\overline{R_e}})(V_{\underline{S}}-\overline{V_{Be}}-\overline{V_A}) - V_{\underline{S}}}{\frac{\overline{R_B}(\overline{R_e}+\overline{R_c})}{\overline{R_e}} + \overline{R_c}}$$

$$\underline{I_{B_{66}}} = \frac{0.5 + 5.46 + (\frac{10+46.4}{10})(11.5-1.5-5.46) - 11.5}{1.03\frac{178(46.4+10)}{10} + 46.4}$$

$$\underline{I_{B_{66}}} = 17.7 \text{ milliamperes}$$

Minimum and Maximum Base Current to Driver

$$\underline{i_{b_{69}}} = \underline{i_{e_{66}}} - \frac{\overline{V_{Be_{69}}}}{\underline{R}}$$

$$\underline{i_{b_{69}}} = 110 - \frac{1.925}{0.97(150)}$$

$$\underline{i_{b_{69}}} = 96.75 \text{ milliamperes}$$

$$\overline{i_{b_{69}}} = \overline{i_{e_{66}}} - \frac{V_{Be_{69}}}{\overline{R}}$$

$$\overline{i_{b_{69}}} = 220 - \frac{0.772}{1.03(150)}$$

$$\overline{i_{b_{69}}} = 215 \text{ milliamperes}$$

Check reverse bias on T_2 of next stage

$$\overline{V_{c_2}} = \overline{V_{Be_{69}}} + \overline{V_{ce_2}} = 1.925 + 0.39 \text{ volts}$$

$$\overline{V_{c_2}} = 2.315 \text{ volts}$$

$$\underline{V_S} = 2.5(0.96) = 2.4 \text{ volts}$$

$$\underline{V_{BT_2}} = \underline{V_S} - \overline{I}_{leakage} \times \overline{R2}$$

$$= 2.4 - (1 \times 10^{-6})(121 \times 10^3)(1.03)$$

$$\underline{V_{BT_2}} = 2.275$$

This also is acceptable since it does not exceed 0.1 volt.

3.3.3.2. A-COUNTER. The operation of the A-counter in the standby state is exactly the same as that of the B-counter. A difference arises between the two counters only during the drive state. In the B-counter it was possible to neglect the amount of current flowing into the gate terminals during the drive state (because only the hold current was flowing). While in the A-counter a maximum worst-case pulse current of 21.6 milliamperes is driven into the gate terminal from the base of the A amplifier while a hard loop current of 14 milliamperes is present. In this case a circuit β less than 6.25 is required (see Figure 47b). These values will be calculated in the following paragraphs. Refer to Figure 44 for the A-counter schematic.

Drive Condition. Equation where applicable will be carried over for the design of the B-counter.

$$\overline{V_A} = \overline{V_D} + \overline{V_{ce}} + \overline{V_{Be}} + \overline{V_D}$$

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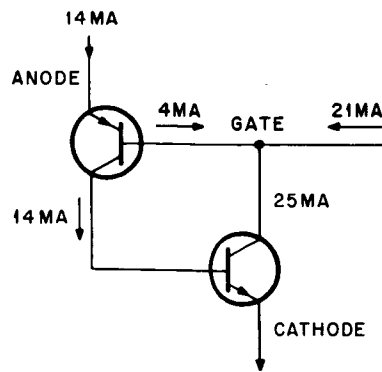
Figure 47b. Basic A-Counter Configuration

$$\overline{v_{Be}} = 1.2(1) + 2.5(50)mv/^{o}C = 1.4 \text{ volts}$$

$$\overline{v_{D}} = 1.2(1) + 2.5(50)mv/^{o}C = 1.4 \text{ volts}$$

$$\overline{v_{ce}} = 1.3(0.38) = 0.5 \text{ volts}$$

$$\overline{V_{A}} = 1.4 + 0.5 + 1.4 + 1.4 = 4.7 \text{ volts}$$

$$\underline{V_{A}} = \underline{V_{D}} + \underline{V_{ce}} + \underline{V_{Be}} + \underline{V_{D}}$$

$$\underline{v_{Be}} = 0.8(0.5) - 2(75)mv/^{o}C = 0.2$$

$$\underline{v_{D}} = 0.8(0.5) - 2(75)mv/^{o}C = 0.2$$

$$\underline{v_{ce}} = 0.9(0.11) = 0.1$$

$$\underline{V_{A}} = 0.2 + 0.1 + 0.2 + 0.2 = 0.8 \text{ volts.}$$

The following equations are carried over from the design of the B-counter.

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$$I_e = \frac{V_S - V_{ce} - V_A + \dfrac{R_c}{R_B}(V_S - V_{Be} - V_A)}{R_e + R_c + \dfrac{R_c}{R_B}(R_e)}$$

$$I_B = \frac{V_{ce} + V_A + \left(\dfrac{R_e + R_c}{R_e}\right)(V_S - V_{Be} - V_A) - V_S}{\dfrac{R_B(R_e + R_c)}{R_e} + R_c}$$

Minimum and Maximum Hard Loop Pulse

$$\overline{I}_e = \frac{\overline{V}_S - \underline{V}_{ce} - \underline{V}_A + \dfrac{R_c}{R_B}(\overline{V}_S - \underline{V}_{Be} - \underline{V}_A)}{\underline{R}_e + \underline{R}_c + \dfrac{R_c}{R_B}\underline{R}_e}$$

using at 20 milliamperes

$$\underline{V}_{ce} = 0$$

$$\underline{V}_{Be} = 0.8(0.9) - 2.5(75 \times 10^{-3}) = 0.53$$

$$\overline{V}_{ce} = 1.3(0.2) = 0.26$$

$$\overline{V}_{Be} = 1.2(1.1) + 2.5(50 \times 10^{-3}) = 1.45$$

$$R_e = 51.1 \text{ ohms}$$

$$R_c = 464 \text{ ohms}$$

$$R_B = 2.37 \text{ kilohms}$$

$$\overline{I_e} = \frac{12.5 - 0 - 0.8 + (\frac{464}{2.37K})(12.5-0.8-0.8)}{0.97\left\{51.1 + 464 + \frac{464}{2.37K}(51.1)\right\}}$$

$$\overline{I_{e_{66}}} = 27.2 \text{ milliamperes}$$

$$\underline{I_e} = \frac{\underline{V_S} - \overline{V_{ce}} - \overline{V_A} + \frac{\overline{R_c}}{R_B}(\underline{V_S}-\overline{V_{Be}}-\overline{V_A})}{\overline{R_e} + \overline{R_c} + \frac{\overline{R_c}}{R_B}R_e}$$

$$\frac{11.5 - 0.26 - 4.7 + \frac{464}{2.37K}(11.5-1.45-4.7)}{1.03\left\{51.1 + 464 + \frac{464}{2.37K}(51.1)\right\}}$$

$$\underline{I_{e_{66}}} = 14.1 \text{ milliamperes}$$

Maximum Possible Current into Gate (Collector T_2)

$$\overline{V_S} = \underline{V_D} + \underline{V_{Be}} + \underline{i}R_{B_{T3}} + \underline{V_{ce}} + \underline{V_D}$$

$$\overline{I_{B_3}} = \frac{\overline{V_S} - (\underline{V_D}+\underline{V_{Be}}+\underline{V_{ce}}+\underline{V_D})}{\underline{R_B}}$$

$$\overline{I_{B_3}} = \frac{12.5 - (0.2+0.2+0.1+0.2)}{0.97(560)} =$$

$$\overline{I_{B_3}} = 21.6 \text{ milliamperes}$$

Minimum and Maximum Load on Input

$$I_B = \frac{\overline{V_{ce}} + \overline{V_A} + (\frac{\overline{R_e} + \overline{R_c}}{\overline{R_e}})(V_S - \overline{V_{Be}} - \overline{V_A}) - V_S}{\frac{\overline{R_B}(\overline{R_e} + \overline{R_c})}{\overline{R_e}} + \overline{R_c}}$$

$$I_B = \frac{0.26 + 4.7 + (\frac{51.1 + 464}{51.1})(11.5 - 1.45 - 4.7) - 11.5}{1.03 \left\{ \frac{2370(51.1 + 464)}{51.1} + 464 \right\}}$$

$$\underline{I_{B_{66}}} = 1.9 \text{ milliamperes}$$

$$\overline{I_B} = \frac{V_{ce} + \underline{V_A} + (\frac{\underline{R_e} + \underline{R_c}}{\underline{R_e}})(\overline{V_S} - V_{Be} - \underline{V_A}) - \overline{V_S}}{\frac{\underline{R_B}(\underline{R_e} + \underline{R_c})}{\underline{R_e}} + \underline{R_c}}$$

$$\overline{I_B} = \frac{0 + 0.8 + (\frac{51.1 + 464}{51.1})(12.5 - 0.53 - 0.8) - 12.5}{0.97 \left\{ \frac{2.37K(51.1 + 464)}{51.1} + 464 \right\}}$$

$$\overline{I_{B_{66}}} = 4.25 \text{ milliamperes}$$

Check reverse bias on T_2 of next stage.

Since the change in V_{C2} during pulse time is not as great as in the B-counter it can be concluded that this part is good. This then completes the design of the A-counter. The driver portion will appear in the line regulation portion since it is so intimately connected to regulation.

3.3.3.3. P-COUNTER AND DRIVER. The operation of the P-counter and driver is basically the same as that of the A-counter and amplifier. The difference

between these two arises in the amount of current that is passed during the pulse state. It was shown for the A-counter that the hold current was 14 milliamperes while the gate current was 21 milliamperes. In the P-counter the minimum anode current is 13 milliamperes while the maximum possible gate current is 12.2 milliamperes. The transistors are the same as those used in the A-counter so that breakdown voltages still apply.

Figure 45 is the schematic of the P-counter.

<u>Drive Condition</u>. Equations where applicable will be carried over from the designs of the A and B drivers.

$$\overline{V_A} = \overline{V_D} + \overline{V_{ce}} + \overline{V_{Be}} + \overline{V_D}$$

$$\overline{v_{Be}} = 1.2(1) + (2.5mv/^oC)(50) = 1.4 \text{ volts}$$

$$\overline{v_D} = 1.2(1) + (2.5mv/^oC)(50) = 1.4 \text{ volts}$$

$$\overline{v_{ce}} = 1.3(0.38) = 0.5$$

$$\overline{V_A} = 1.4 + 0.5 + 1.4 + 1.4 = 4.7 \text{ volts}$$

$$\underline{V_A} = \underline{V_D} + \underline{V_{ce}} + \underline{V_{Be}} + \underline{V_D}$$

$$\underline{v_D} = 0.8(0.5) - (2.5mv/^oC)(75) = 0.2 \text{ volts}$$

$$\underline{v_{Be}} = 0.8(0.5) - (2.5mv/^oC)(75) = 0.2 \text{ volts}$$

$$\underline{v_{ce}} = 0.9(0.11) = 0.1 \text{ volts}$$

$$\underline{V_A} = 0.2 + 0.1 + 0.2 + 0.2 = 0.7 \text{ volts}$$

The following equations are carried over from the design of the B-counter.

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$$I_e = \frac{V_S - V_{ce} - V_A + \dfrac{R_c}{R_B}(V_S - V_{Be} - V_A)}{R_e + R_c + \dfrac{R_c}{R_B} R_e}$$

$$I_b = \frac{V_{ce} + V_A + (\dfrac{R_e + R_c}{R_e})(V_S - V_{Be} - V_A) - V_S}{\dfrac{R_B(R_e + R_c)}{R_e} + R_c}$$

Minimum and Maximum Hard Loop Pulse

$$\overline{I_e} = \frac{\overline{V_S} - \underline{V_{ce}} - \underline{V_A} + \dfrac{R_c}{\overline{R_B}}(\overline{V_S} - \underline{V_{Be}} - \underline{V_A})}{\underline{R_e} + \underline{R_c} + (\dfrac{R_c}{\overline{R_B}})\,\underline{R_e}}$$

using at 20 milliamperes

$$\underline{v_{ce}} = 0$$

$$\underline{v_{be}} = 0.8(0.9) - (2.5 \text{ mv/}^{o}\text{C})(75) = 0.53$$

$$\overline{v_{Ce}} = 1.3(0.2) = 0.26$$

$$\overline{v_{Be}} = 1.2(1.1) + (2.5 \text{ mv/}^{o}\text{C})(50) = 1.45$$

$$R_e = 61.9 \text{ ohms}$$

$$R_c = 511 \text{ ohms}$$

$$R_B = 2.05 \text{ kilohms}$$

$$\overline{I_e} = \frac{12.5 - 0 - 0.8 + \frac{511}{2050}(12.5 - 0.8 - 0.8)}{0.97(61.9 + 511 + \frac{511}{2.05K} \times 61.9)}$$

$$\overline{I_{e_{66}}} = 24.3 \text{ milliamperes}$$

$$\underline{I_e} = \frac{\underline{V_S} - \overline{V_{ce}} - \overline{V_A} + \frac{\overline{R_c}}{\overline{R_B}}(\underline{V_S} - \overline{V_{Be}} - \overline{V_A})}{\overline{R_e} + \overline{R_c} + (\frac{\overline{R_c}}{\overline{R_B}})\overline{R_e}}$$

$$\underline{I_e} = \frac{11.5 - 0.26 - 4.7 + \frac{511}{2050}(11.5 - 1.45 - 4.7)}{1.03(61.9 + 511 + \frac{511}{2050} \times 61.9)}$$

$$\underline{I_e} = 13 \text{ milliamperes}$$

Maximum Possible Current into Gate (Collector T_2)

$$\overline{I_{B_3}} = \frac{\overline{V_S} - (\underline{V_D} + \underline{V_{Be}} + \underline{V_{ce}} + \underline{V_D})}{\underline{R_B}}$$

$$\overline{I_{B_3}} = \frac{12.5 - (0.2 + 0.2 + 0.1 + 0.2)}{0.97(1000)}$$

$$\overline{I_{B_3}} = 12.2 \text{ milliamperes}$$

$$I_B = \frac{\overline{V_{ce}} + \overline{V_A} + (\frac{\overline{R_e} + \overline{R_c}}{\overline{R_e}})(V_S - \overline{V_{Be}} - \overline{V_A}) - V_S}{\frac{\overline{R_B}(\overline{R_e} + \overline{R_c})}{\overline{R_e}} + \overline{R_c}}$$

$$I_B = \frac{0.26 + 4.7 + (\frac{61.9 + 511}{61.9})(11.5 - 1.450 4.7) - 11.5}{1.03 \left\{ \frac{2050(61.9 + 511)}{61.9} + 511 \right\}}$$

$$I_B = 2.14 \text{ milliamperes}$$

$$\overline{I_B} = \frac{V_{ce} + V_A + (\frac{R_e + R_c}{R_e})(\overline{V_S} - V_{Be} - V_A) - \overline{V_S}}{\frac{R_B(R_e + R_c)}{R_e} + R_c}$$

$$\overline{I_B} = \frac{0 + 0.8 + (\frac{61.9 + 511}{61.9})(12.5 - 0.53 - 0.8) - 12.5}{0.97 \left\{ \frac{2050(51.9 + 511)}{61.9} + 511 \right\}}$$

$$\overline{I_B} = 4.8 \text{ milliamperes}$$

$$I_{B_3} = \frac{V_{in} - (\overline{V_D} + \overline{V_{BeT_3}} + \overline{V_{Ce}} + \overline{V_D})}{\overline{R_B}}$$

$$I_{B_3} = \frac{11.5 - (1.4 + 1.4 + 0.5 + 1.4)}{1.03(1000)}$$

$$I_{B_3} = 6.6 \text{ milliamperes}$$

Since maximum load 60 milliamperes

therefore required $\beta = 9.1$

therefore initial room temperature $\beta = \dfrac{9.1}{0.6 \times 0.66} = 23$

3.3.3.4. GATE CIRCUIT. Figure 48 is a partial schematic of the interconnection of the gate circuits to the counters. Since in the schematic the P-counter has the largest amount of loading, it will be necessary to check this circuit only.
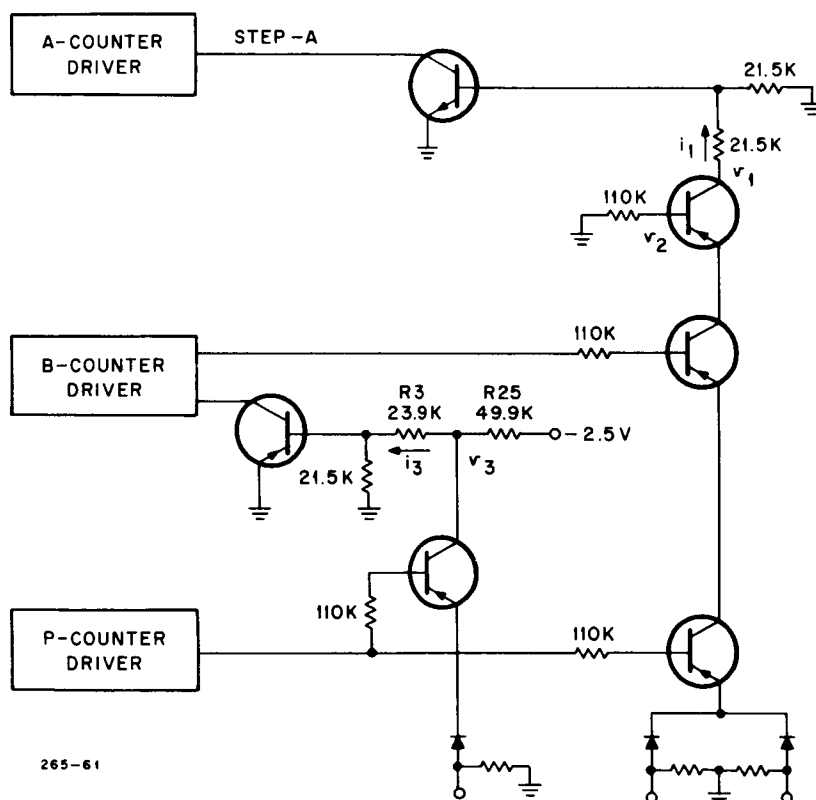
Figure 48. Step Gate

Step A-Counter

$$i_{b5} = \frac{250\mu a}{10} = 25 \text{ microamperes}$$

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$$\underline{v}_1 = \underline{V}_S - (4\overline{V_T} + \overline{V_D})$$

$$\overline{V_D} = 1.2(0.5) + (2.5mv/^oC)(50^oC) \% \ 0.6 + 0.125 = 0.725$$

$$\underline{V}_S = 5 \times 0.96 = 4.8 \text{ volts} \quad \overline{V_S} = 5 \times 1.04 = 5.2 \text{ volts}$$

$$\underline{V}_1 = 4.8 - (4\times0.3+0.8) = 2.8 \text{ volts}$$

$$\overline{i_{BIAS5}} = \frac{\overline{v_{Be}}}{\underline{R}} = \frac{1}{(2.15\times10^3)(0.97)} = 48 \text{ microamperes}$$

$$\underline{i}_1 = i_{BIAS_5} + \underline{i}_{b_5} = 48 + 25 = 73 \text{ microamperes}$$

$$\overline{R} = \frac{\underline{V}_1 - \overline{V_{Be}}}{\underline{i}_1} = \frac{2.8 - 1}{73 \times 10^{-6}} = 24.6 \text{ kilohms}$$

if use 21.5 kilohms,   therefore $\overline{R} = 1.03(21.5K) = 22.2$ kilohms

$$\overline{i_1} = \frac{\overline{V_S} - (4\underline{V_{ce}} + \underline{V_D} + \underline{V_{Be}})}{\underline{R}}$$

$$\overline{i_1} = \frac{5.2 - (4\times0.1+0.15+0.15)}{0.97(21.5K)} = 216 \text{ microamperes}$$

using a derated B = 12

$$\underline{i}_b = \frac{216}{12} = 18 \text{ microamperes}$$

$$\underline{v}_2 - \underline{v}_S - (\overline{V_D} + 3\overline{V_{ce}} + \overline{V_{Be}})$$

$$\overline{v_{Be}} = 1.2(0.7) + (2.5mv/^oC)(50) = 0.8 + 0.12 = 0.92$$

use 0.95

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$$\overline{v_{ce}} = 0.23 \times 1.2 = 0.276 \qquad \text{use } 0.28 \text{ volts}$$

$$\underline{V_2} = 4.8 - (0.8 + 3(0.28) + 0.95) = 2.2 \text{ volts}$$

$$\overline{R_2} = \frac{V_2}{\underline{i_b}} = \frac{2.2}{18 \times 10^{-6}} = 122 \text{ kilohms} \qquad \text{use } 110 \text{ kilohms}$$

therefore actual

$$\underline{i_b} = \frac{V_2}{\overline{R_2}} = \frac{2.2}{1.03(110 \times 10^3)} = 19.4 \text{ microamperes}$$

$$\overline{i_b} = \frac{\overline{V_S} - (\overline{V_{ce}} + \underline{V_D} + \underline{V_{Be}})}{\underline{R}}$$

$$\overline{i_b} = \frac{5.2 - (0.1 + 0.1 + 0.1)}{0.97(110K)} = 46 \text{ microamperes}$$

$$\overline{i_{in}} = 3(\underline{i_b} + i_1) = 3(46 \times 10^{-6}) + 216 \times 10^{-6} = 354 \text{ microamperes}$$

Since the maximum base current is 46 microamperes the P-counter will have a load of 92 microamperes maximum. Since this current is flowing into the gate terminal of the counter we will check the new β requirement. See Figure 49, the simplified schematic with new current values, and assume the currents split as shown. The circuit β would be required to be;
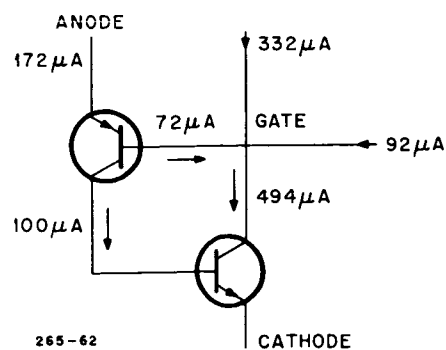
Figure 49. Basic Counter

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$$\frac{494}{100} \times \frac{100}{72} = 6.85$$

This is still much smaller than the available transistor β.

<u>Step B-Counter</u>. Refer back to Figure 48 and allow maximum i_1 equal i_3 therefore

$$R3 = \frac{\overline{V_S} - (2V_{ce} + V_D + V_{Be})}{\overline{i_1}}$$

$$\underline{R3} = \frac{5.2 - (2 \times 0.1 + 0.15 + 0.15)}{216 \times 10^{-6}}$$

$\underline{R3}$ = 21.8 kilohms   use 23.7 kilohms   therefore $\underline{R}$ = 23 kilohms

Check i_3 minimum

$$\underline{V_3} = \underline{V_S} - (2\overline{V_{ce}} + \overline{V_D})$$

$$\underline{V_3} = 4.8 - (2 \times 0.3 + 0.8) = 3.8$$

$$\underline{i_3} = \frac{\underline{V_3} - \overline{V_{Be}}}{\overline{R}} = \frac{3.8 - 1}{1.03(23.7 \times 10^3)} = 117 \text{ microamperes}$$

$$\overline{v_3} = \overline{V_S} - (\underline{V_D} + \underline{V_T})$$

$$= 5.2 - (0.1 + 0.1) = 5 \text{ volts}$$

$$\overline{i_{R25}} = \frac{5 + 2.5(1.04)}{(0.97)(49.9)} = \frac{7.6}{48.5} = 156.5 \text{ microamperes}$$

$$\overline{i_{in}} = \overline{i_b} + \overline{i_{R25}} + \overline{i_3} = 46 + 156.5 + 216$$

$$\overline{i_{in}} = 418.5 \text{ microamperes.}$$

3.3.3.5. CLEAR AND SET CIRCUITS. Figure 50 is a schematic showing the interconnection of the clear circuits.
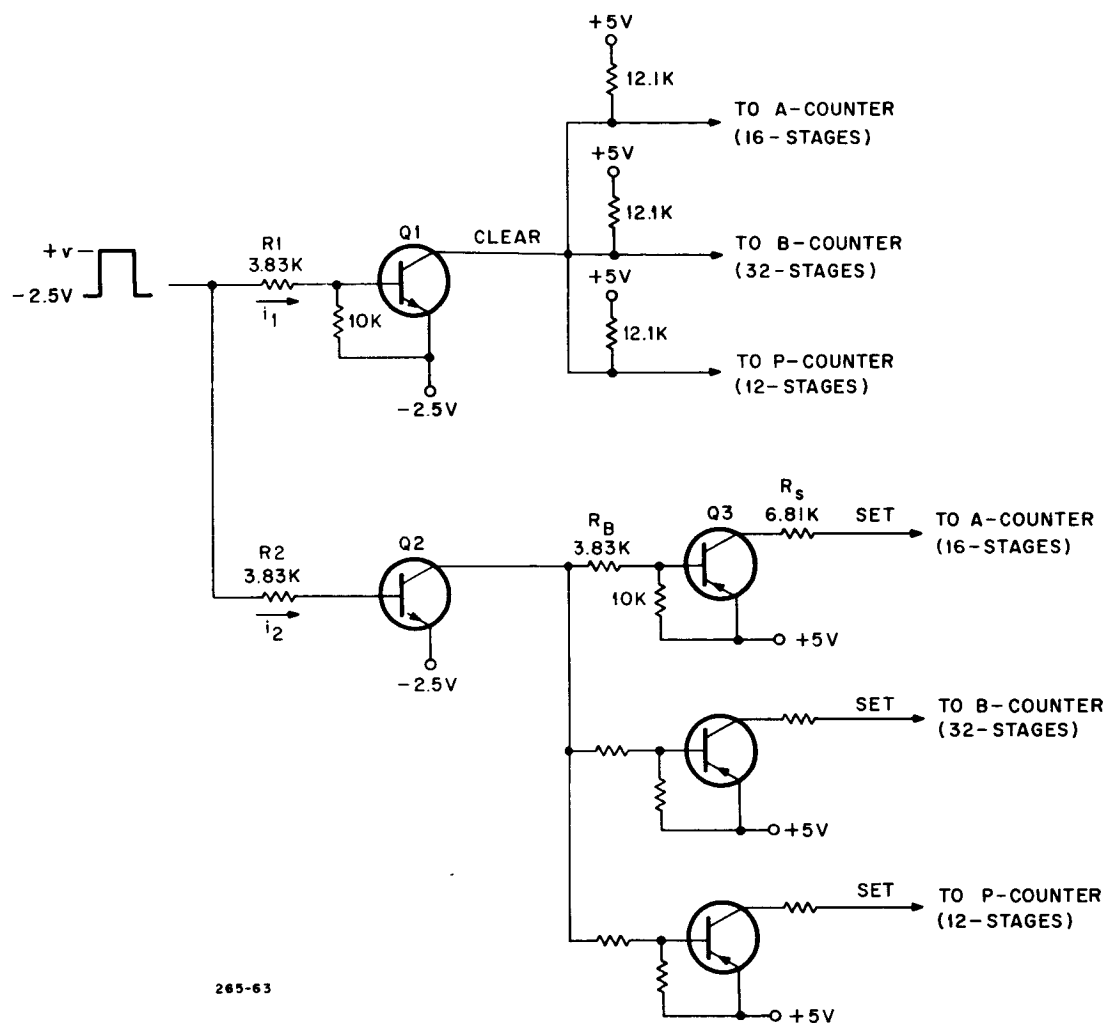
Figure 50. Set and Clear Circuits

Clear Circuits. The clear signal must be able to clear the A-, B-, and P-counters. First let us calculate the resistor value for R_c

leakage of 60 diodes   = 600 microamperes

leakage of 3 transistors = $\underline{\hspace{0.1cm}30\hspace{0.1cm}}$ microamperes
$\hspace{5.5cm}$ 630 microamperes

Allow the voltage on the hold-off resistor to go from +5 to +2.5

therefore,

$$\overline{R} = \frac{2.5}{0.63 \times 10^{-3}} = 3.97 \text{ kilohms}$$

when using a split load 3×3.97 kilohms = 11.8 kilohms   use 12.1 kilohms

$$\overline{i_{BIAS}} = \frac{\overline{V_{CC}} + \overline{V_E}}{\underline{R}} = \frac{(5+2.5)1.04}{(\frac{12.1K}{3})(0.97)} = 2 \text{ milliamperes}$$

and allow 1 milliampere to clear the counters

therefore,

$$\overline{i} = 3 \text{ milliamperes and } \underline{i_b} = 0.3 \text{ milliamperes}$$

$$\overline{i_{BIAS}} = \frac{\overline{V_{BE}}}{(10 \times 10^3)(0.97)} = 1.03 \text{ milliamperes}$$

$$i_1 = i_{BIAS} + i_b$$

$$= 1.03 + 0.3 = 1.4 \text{ milliamperes}$$

$$\overline{R1} = \frac{(V_{in} + \overline{V_E}) - (\overline{V_{BE}} + \overline{V_{ce}})}{\underline{i_1}}$$

$$\overline{R1} = \frac{7.5 \times 0.96 - (1+0.5)}{1.4 \times 10^{-3}} = 4.06 \text{ kilohms}$$

use 3.83 kilohms

$$\overline{i_1} = \frac{(\overline{V_{in}} + \overline{V_E}) - (\underline{V_{Be}} + \underline{V_{ce}})}{\underline{R1}}$$

$$\overline{i_1} = \frac{(7.5 \times 1.04) - 0}{3.83(0.97) \times 10^3} = 2.1 \text{ milliamperes}$$

Since the maximum load on the input will be twice this current, the maximum loading on the input signal will be 4.2 milliamperes.

Set Circuits. The set circuits must be able to set the A-, B-, and P-counters. Each counter has its own transistor buffer, as shown in Figure 50.

Allow 0.5 milliampere to set a counter

$$\overline{R_S} = \frac{V_S - V_{counter}}{i} = \frac{5(0.96) - 1.2}{0.5}$$

$$\overline{R_S} = 7.2 \text{ kilohms} \quad \text{use } 6.81 \text{ kilohms}$$

$$i_b = \frac{0.5 \times 10^{-3}}{10} = 50 \text{ microamperes}$$

$$\overline{i_{BIAS}} = 1.03 \text{ milliamperes}$$

$$i = 1.03 + 0.050 = 1.1 \text{ milliampere}$$

$$\overline{R_B} = \frac{V_{S_1} + V_{S_2} - (\overline{V_{ce}} + \overline{V_{Be}})}{1.1} = \overline{R_B} = \frac{7.2 - (1+0.5)}{1.1} = 5.2 \text{ kilohms}$$

use 3.83 kilohms

$$\overline{i} = \frac{7.5 \times 1.04}{3.83 \times 0.97} = 2.1 \text{ milliamperes}$$

$$\overline{3i} = 6.3 \text{ milliamperes}$$

$$i_2 = \frac{V_{S_1} + V_{S_2} - (\overline{V_{ce}} + \overline{V_{BE}})}{\overline{R2}}$$

$$= \frac{7.2 - (1.5)}{1.03(3.83K)} = 1.45 \text{ milliamperes}$$

Therefore β required $= \dfrac{6.3}{1.45} = 4.35$

3.3.3.6. COLLECTOR AND BASE REGULATOR. This section shows the calculations for the collector and base regulator circuits. The configurations of these circuits are typical with the exception of pulsing the circuit on and off. Figure 51 shows the interconnection of the circuits to the word line. Since the current tolerance required of the regulator is tight compared to logic
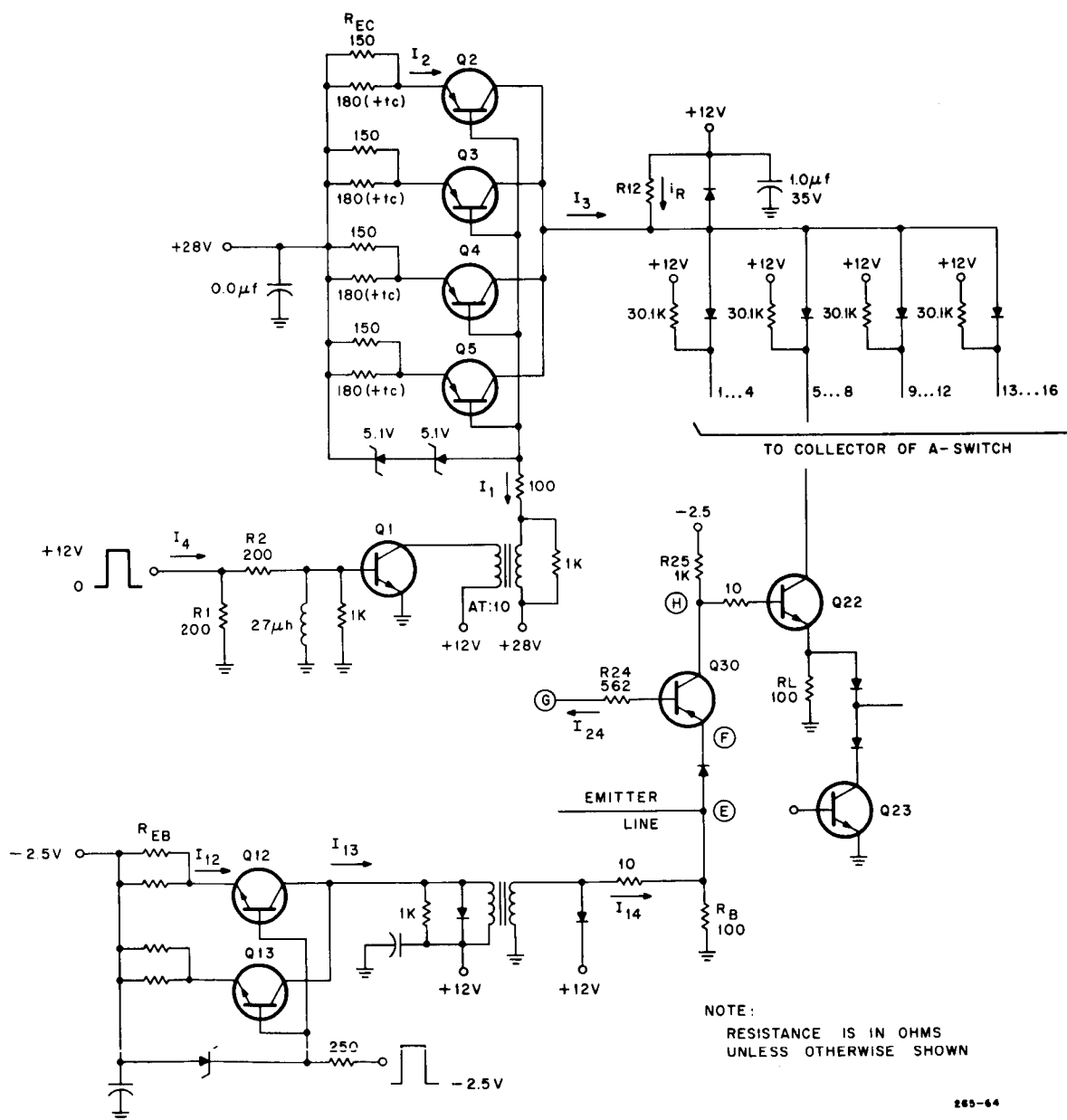
Figure 51.   Base and Collector Regulators

circuits and since current is adjusted to the optimum operating point, the initial tolerance of the components will not be included in this calculation. The word drive current is changed inversely as a function of temperature by the positive temperature coefficient resistors in the emitters of Q2, Q3, Q4, and Q5 (Figure 51). The measured word drive current as a function of temperature is approximately -0.15 percent.

$$-20^{\circ}C \qquad 785 \text{ ma}$$

$$+25^{\circ}C \qquad 735 \text{ ma}$$

$$+50^{\circ}C \qquad 707 \text{ ma}$$

To calculate the maximum loading on the input:

$$I_4 = \frac{\overline{V_{in}} - V_{BE_{T1}}}{\underline{R2}} + \frac{V_{in}}{\overline{R2}}$$

assume $V_{Be} = 0$

$$I_4 = \frac{12}{100} = 120 \text{ milliamperes}$$

To calculate the variation in I_3 it will be assumed that the forward impedance of the Zener diodes is zero. This assumption is valid because the current I_1 is great enough to drive the Zener diode into a very low impedance level.

Source Stiffness

Therefore
$$i_2 = \frac{V_Z - V_{Be_{T2}}}{R_{EC}}$$

allow

$\overline{V_Z} = 10.4 \text{ volts}$ $\overline{V_{BE}} = 1.1 \text{ volts}$

$\underline{V_Z} = 10.0 \text{ volts}$ $\underline{V_{BE}} = 0.9 \text{ volts}$

$$R_{EC} = \frac{130 \times 180}{310} = 75.5 \text{ ohms}$$

$$\overline{i_2} = \frac{V_Z - \underline{V_{Be}}}{\underline{R_{EC}}} = \frac{10.4 - 0.9}{75.5(0.99)} = 127 \text{ milliamperes}$$

$$\underline{i_2} = \frac{V_Z - \overline{V_{BE}}}{\overline{R_{EC}}} = \frac{10 - 1.1}{75.5(1.01)} = 117 \text{ milliamperes}$$

variation (10 milliamperes)

Now it is necessary to allow for a transistor h_{FE} variation. If the transistors are selected for a h_{FE} of 150—250 at I_c = 110 milliamperes and V_{CE} out of saturation (10 volts) the following equations apply:

$$\underline{h_{FE}} = 150 \times 0.7 = 105.0$$

$$\overline{h_{FE}} = 250 \times 1.2 = 300$$

Therefore,

$$\underline{\alpha} = \frac{\underline{h_{FE}} - 1}{\underline{h_{FE}}} = \frac{104}{105} = 0.990$$

$$\overline{\alpha} = \frac{\overline{h_{FE}} - 1}{\overline{h_{FE}}} = \frac{299}{300} = 0.996$$

$$\overline{i_3} = 4(0.996)(127) = 505 \text{ milliamperes}$$

$$\underline{i_3} = 4(0.99)(117) = 465 \text{ milliamperes}$$

Nominal i_3 = 485

Variation (40 milliamperes)

150

Current from 33 ohms Damping Resistor (R12)

$$\overline{V_D} = 1.3 + 0.1 = 1.4 \qquad \underline{V_D} = 1.1 - 0.1 = 1.0$$

$$\overline{V_{CE}} = 0.9 + 0.1 = 1.0 \qquad \underline{V_{Ce}} = 0.6 - 0.1 = 0.5$$

$$i_R = \frac{V_S - (3V_D + 2V_{CE})}{R12}$$

$$\underline{i_R} = \frac{\underline{V_S} - (3\overline{V_D} + 2\overline{V_{CE}})}{\overline{R12}}$$

$$\overline{i_R} = \frac{\overline{V_S} - (3\underline{V_D} + 2\underline{V_{CE}})}{\underline{R12}}$$

$$\underline{i_R} = \frac{11.5 - (3 \times 1.4 + 2 \times 1)}{33(1.01)} = \frac{11.5 - 6.2}{50.5}$$

$$\underline{i_R} = 159 \text{ milliamperes}$$

$$\overline{i_R} = \frac{12.5 - (3+1)}{33(0.99)} = \frac{12.5 - 4}{49.5}$$

$$\overline{i_R} = 260 \text{ milliamperes}$$

Nominal i_R = 209 milliamperes

Variation = 100 milliamperes

Current Shunted by 100 ohms Damping Resistor (R_L)

$$\overline{V_{DL}} = 1.4 \qquad\qquad \underline{V_{DL}} = 1.0$$

$$\overline{V_{CE}} = 1.0 \qquad\qquad \underline{V_{CE}} = 0.5$$

$$i_R = \frac{-(2V_{DL} + V_{CE})}{R_L}$$

$$\underline{i_R} = \frac{2V_{DL} + V_{CE}}{\overline{R_L}} = \frac{2 + 0.5}{101} = -24.8 \text{ milliamperes}$$

$$\overline{i_R} = \frac{2\overline{V_{DL}} + \overline{V_{CE}}}{\underline{R_L}} = \frac{2.8 + 1}{99} = -38.4 \text{ milliamperes}$$

Nominal i_{R_L} = 31.6 milliamperes

Variation = 15.6 milliamperes

<u>Base Regulator</u>. The same assumptions as used for the collector regulator will be carried over to the base regulator.

<u>Source Stiffness</u>

$$i_2 = \frac{V_Z - V_{BE_{T12}}}{R_{EB}}$$

allow

$$\overline{V_Z} = 5.2 \qquad\qquad \overline{V_{BE}} = 1.1$$

$$\underline{V_Z} = 5.0 \qquad\qquad \underline{V_{BE}} = 0.9$$

$$\overline{i_{12}} = \frac{\overline{V_Z} - \underline{V_{BE}}}{\underline{R_{EB}}} = \frac{5.2 - 0.9}{20(0.99)} = 217$$

$$\underline{i_{12}} = \frac{\underline{V_Z} - \overline{V_{BE}}}{\overline{R_{EB}}} = \frac{5 - 1.1}{20(1.01)} = 193$$

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Nominal = 205 milliamperes

Variation = 24 milliamperes

Now it is necessary again to allow for a transistor h_{FE} variation. If the transistor is selected for a h_{FE} of 50—100 at I_c = 200 milliamperes and V_{CE} out of saturation (10 volts) the following equations apply.

$$\underline{h_{FE}} = 50 \times 0.7 = 35$$

$$\overline{h_{FE}} = 100 \times 1.2 = 120$$

$$\underline{a} = \frac{\underline{h_{FE}} - 1}{\underline{h_{FE}}} = \frac{34}{35} = 0.97$$

$$\overline{a} = \frac{\overline{h_{FE}} - 1}{\overline{h_{FE}}} = \frac{119}{120} = 0.99$$

$$\overline{i_{14}} = (0.99)(217) = 215 \text{ milliamperes}$$

$$\underline{i_{14}} = (0.97)(193) = 187 \text{ milliamperes}$$

Nominal i_{14} = 201 milliamperes

Variation = 28 milliamperes

Current Shunted by 100 Ohms Base Damper (R_B)

$\begin{matrix} T_{22} \\ T_{23} \end{matrix}$

$$\overline{V_{DL}} = 1.3 + 0.1 = 1.4 \qquad \underline{V_{DL}} = 1.1 - 0.1 = 1.0$$

$$\overline{V_{CEL}} = 0.9 + 0.1 = 1.0 \qquad \underline{V_{CE}} = 0.6 - 0.1 = 0.5$$

$$\overline{V_{BEL}} = 1.8 + 0.2 = 2.0 \qquad \underline{V_{BE}} = 1.4 - 0.15 = 1.25$$

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$$\overline{V_{CE}} = 0.3 + 0.1 = 0.4 \qquad \underline{V_{CE}} = 0.1$$

T_{30}

$$\overline{V_{BE}} = 1.0 + 0.1 = 1.1 \qquad \underline{V_{BE}} = 0.8 - 0.1 = 0.7$$

$$\overline{V_{DE}} = 1.05(1.2) = 1.3 \qquad \underline{V_{DE}} = 0.8(0.9) = 0.72$$

$$V_E = V_{CEL} + 2V_{DL} + V_{BEL} + V_{CE30} + V_{DE} + iR10$$

$$\overline{I_{R_B}} = \frac{\overline{V_{CEL}} + \overline{2V_{DL}} + \overline{V_{BEL}} + \overline{V_{Ce30}} + \overline{V_{DE}}}{\underline{R_B}}$$

$$\overline{I_{R_B}} = \frac{1 + 2.8 + 2 + 0.4 + 1.3}{99} = \frac{7.5}{99}$$

$$\overline{I_{R_B}} = 76 \text{ milliamperes}$$

$$\underline{I_{R_B}} = \frac{0.5 + 2 + 1.25 + 0.1 + 0.72}{101} = \frac{4.57}{101}$$

$$\underline{I_{R_B}} = 45.2 \text{ milliamperes}$$

Nominal = 60.6 milliamperes

Variation = 31.8 milliamperes

Current for A Amplifier (I_{24})

$$I_{24} = \frac{V_F - V_{BE30} - V_G}{R24}$$

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Since this effect will be small assume V_G is zero.

$$\overline{I_{24}} = \frac{\overline{V_F} - V_{BE30}}{\underline{R24}} = \frac{6.2 - 0.7}{562(0.99)} = \frac{5.5}{556}$$

$$\overline{I_{24}} = 9.9 \text{ milliamperes}$$

$$\underline{I_{24}} = \frac{V_F - \overline{V_{BE30}}}{\overline{R24}} = \frac{3.85 - 1.1}{562(1.01)} = \frac{2.75}{567}$$

$$\underline{I_{24}} = 4.85 \text{ milliamperes}$$

Nominal = 7.5 milliamperes

Variation = 5 milliamperes

Current Drawn by Back Bias Resistor (R25)

$$V_A = V_{CEL} + 2V_{DL} + V_{BE2}$$

$$\overline{V_H} = 1.0 + 2.8 + 2.0 = 5.8 \text{ volts}$$

$$\underline{V_H} = 0.5 + 2.0 + 1.25 = 3.75 \text{ volts}$$

$$I_{25} = \frac{V_H - V_{25}}{R25}$$

$$\overline{I_{25}} = \frac{5.8 + 2.5}{0.99K} = 8.4 \text{ milliamperes}$$

$$\underline{I_{25}} = \frac{3.75 + 2.5}{1.01K} = 6.2 \text{ milliamperes}$$

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Nominal = 7.3 milliamperes

Variation = 2.2 milliamperes

Total Current Variation	Nominal		Variation	% Variation
	+	−		
(a) Collector Regulator	485		41	±2.600
(b) 33-ohm damping resistor	209		100	±6.350
(c) 100-ohm damper		31.6	15.6	±0.990
(d) Base Regulator	201		28	±1.780
(e) Base damper		60.6	31.8	±2.020
(f) Amplifier current		7.5	5.0	±0.318
(g) Back bias resistor		7.3	2.2	±0.140
	895	107	2 223.6	14.198
	−107		111.8	
	788 ma			

percent variation = ±14.2 percent.

It is noticed that this variation is greater than the allowable variation of the schmoo plot (refer to Figure 60). When the schmoo plot is taken, part of this 14.2-percent variation is included due to the fact that all lines are not receiving the same currents. In the delivered memory the variation between lines was noted to be approximately 5 percent. Another factor that should be taken into account is that this worst-case calculation summed all of the changes to give this number. It is most unlikely that this many parameters will go to their worst-case values simultaneously. If improvement in the current tolerance would be necessary, the greatest correction could be made in increasing the value of the damping resistors. Another factor that was found to be better than the assumed calculated variation was the power supply distribution. The distribution used in the calculation was 4 percent.

3.4. POWER SUPPLY

Three power supplies have been received and tested by UNIVAC in accordance with the power supply specification, which comprises Appendix VI. The first supply was rejected and returned as a defective unit. The second supply was rejected and returned since it failed to meet the regulation and input power requirements. The third supply met the specification between

+10°C and +50°C but stopped functioning below +10°C. The test data is also given in Appendix VI. The third power supply is mounted in the memory, and provisions for operating the memory from external power supplies have been provided for operation below +10°C. Figures 52, 53, and 54 show energy and power for various operating conditions of repetition rate and temperature.
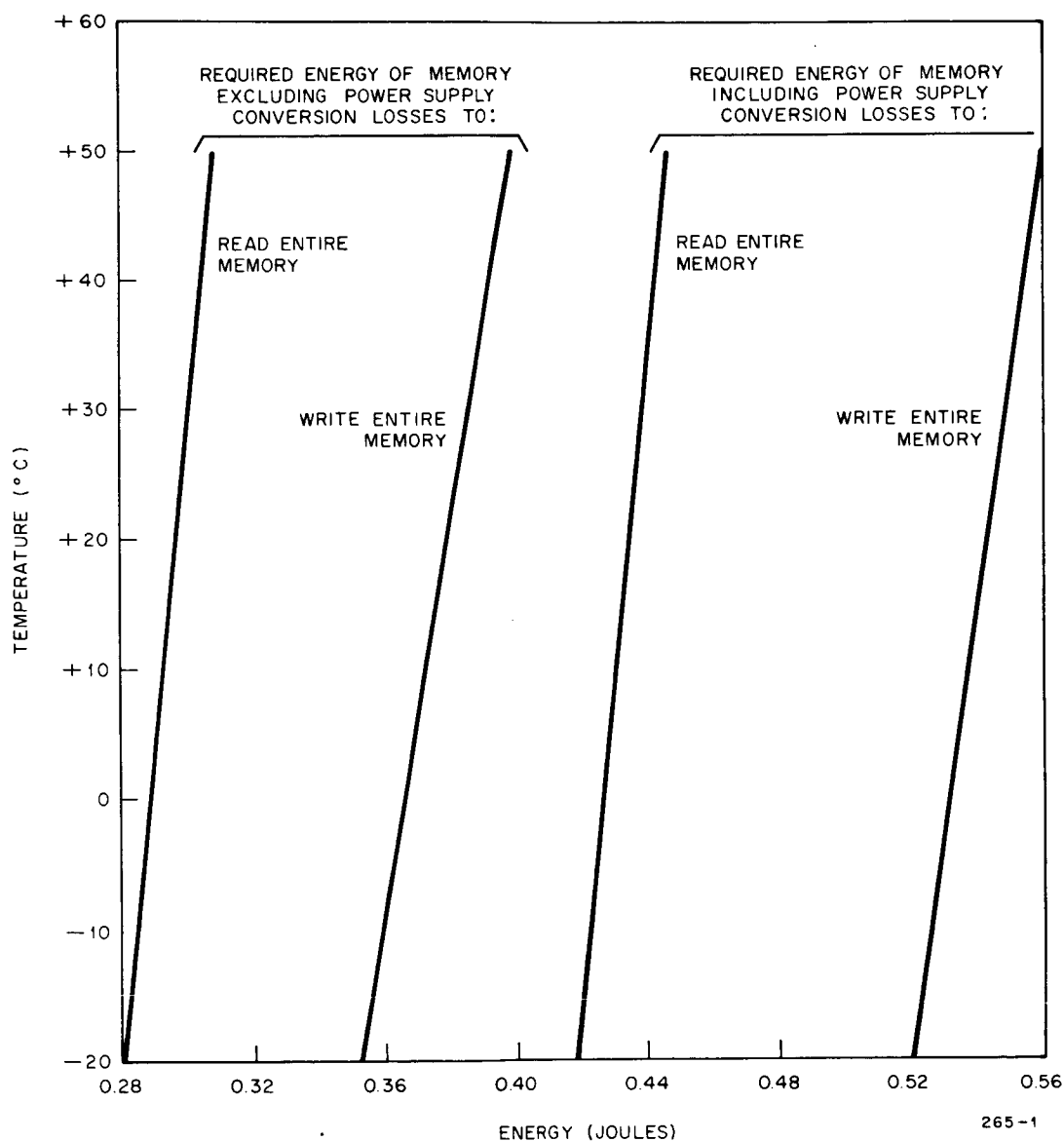
Figure 52. Energy Versus Temperature to Read or
Write Entire Buffer Memory
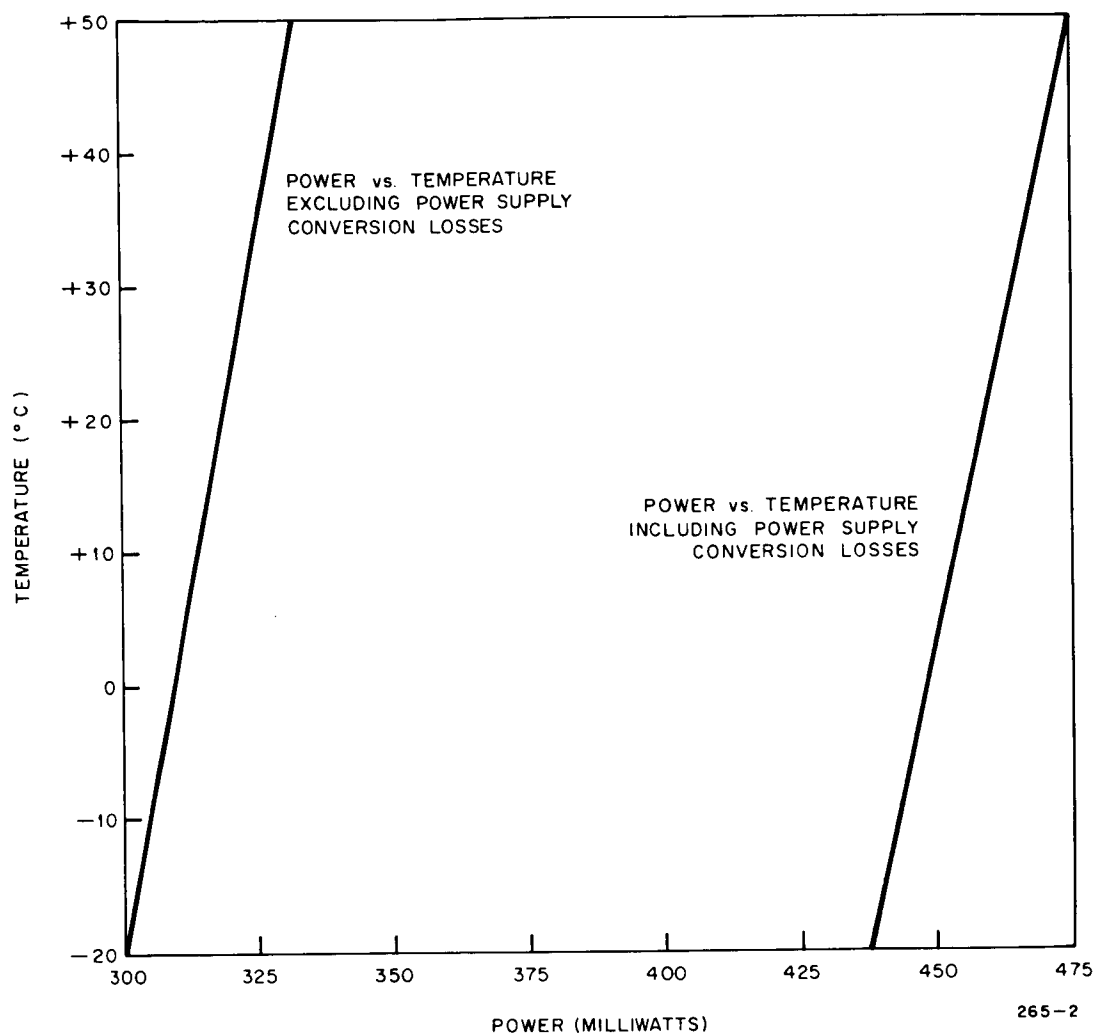
Figure 53. Power Consumption Versus Temperature for Buffer
Memory Measured at 100 Kilocycles Per Second

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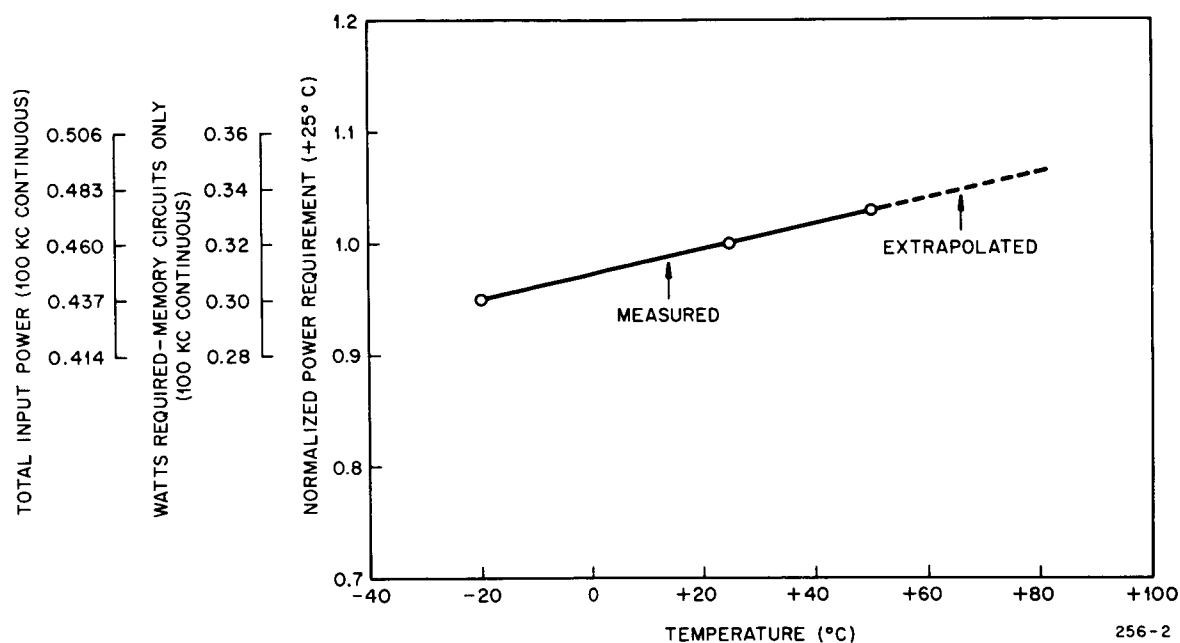
Figure 54.   Power Consumption Versus Temperature for 100,000-
Bit Plated-Wire Memory - 100KC Continuous Operation.   Write then
Read Three Times.

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SECTION 4

MEMORY PACKAGING AND CONSTRUCTION

4.1. CIRCUIT MODULES

Figures 55 through 59 are photographs showing various views of the memory delivered to NASA Goddard Space Flight Center. The memory consists of a total of 186 circuit modules. Many different construction techniques were considered before selection of a final technique. The technique selected depended on the ability of the module to satisfy the following requirements:

1. Be able to contain all the components in the smallest practicable volume.

2. Be able to be freely removed from and reinserted into the backboard.

3. Be repairable at component level before encapsulation.

4. Be rugged enough to withstand vigorous handling during engineering development and testing of memory.

5. Be convertible to modules able to withstand the rigors of launching into outer space.

The minimum volume requirement eliminated conventional mounting to printed-wiring boards. The use of discrete components dictated the use of cordwood construction. In a choice between vertically mounted components and horizontally mounted components, horizontal mounting of components offered an overall volume advantage in system packaging.

The requirement of freely inserting and removing the modules restricted the design to a limited number of choices in commercially available hardware. Available two-piece headers and intermating connectors added unnecessary volume to the system and did not provide convertibility to a flight model without significant engineering changes.
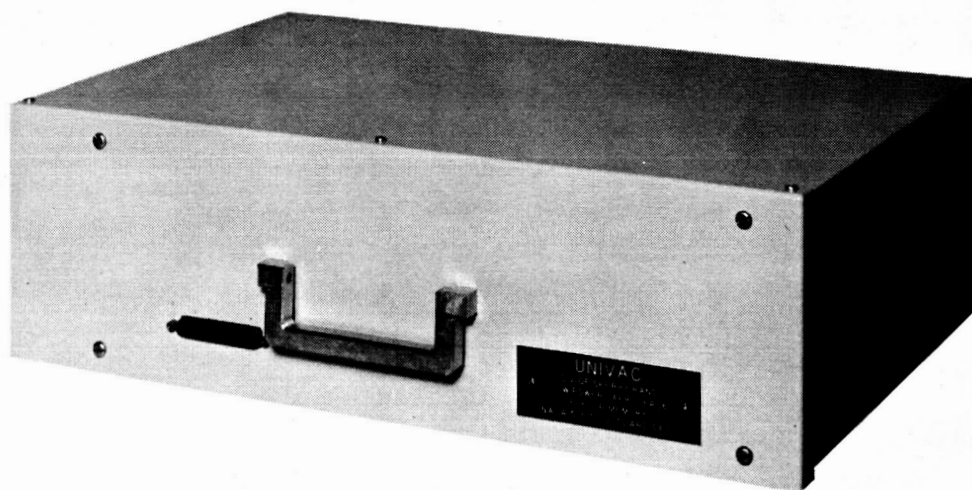
265-45

Figure 55. View Showing Aerospace Memory Package

265-46
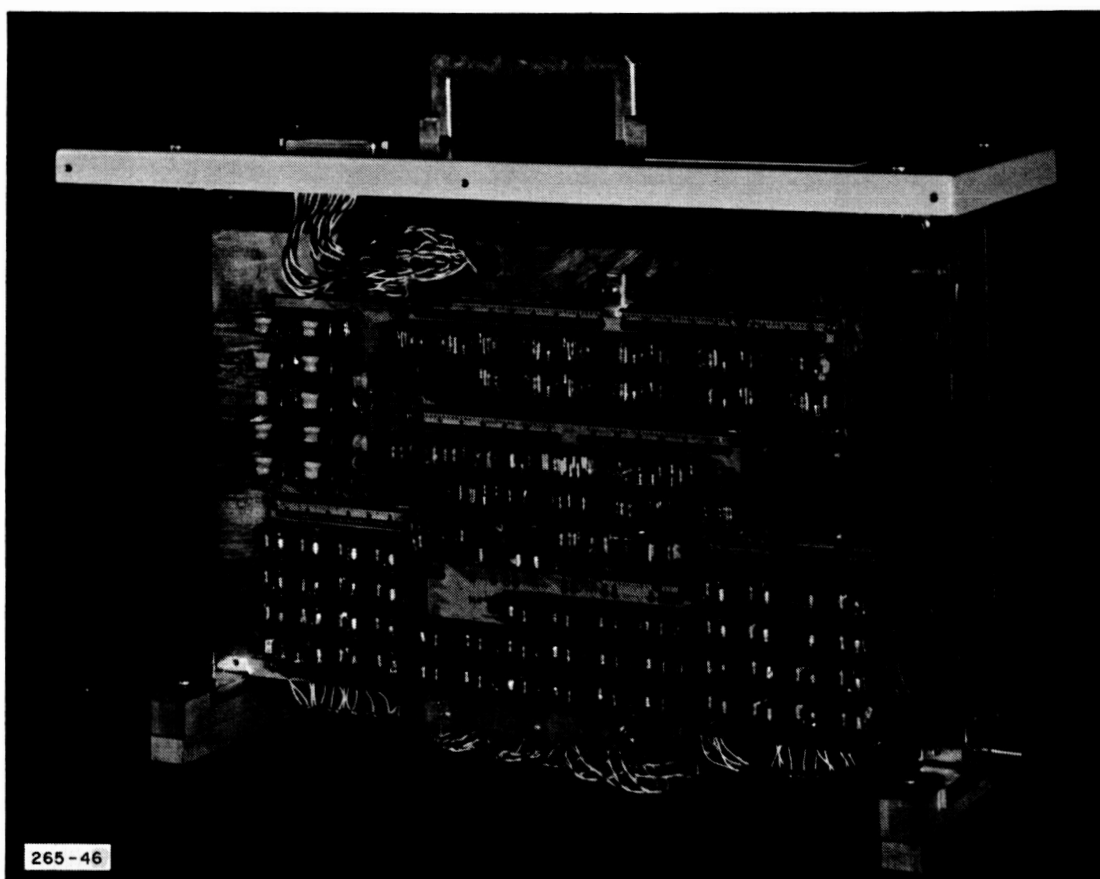
Figure 56. View Showing Timing and Control Circuitry

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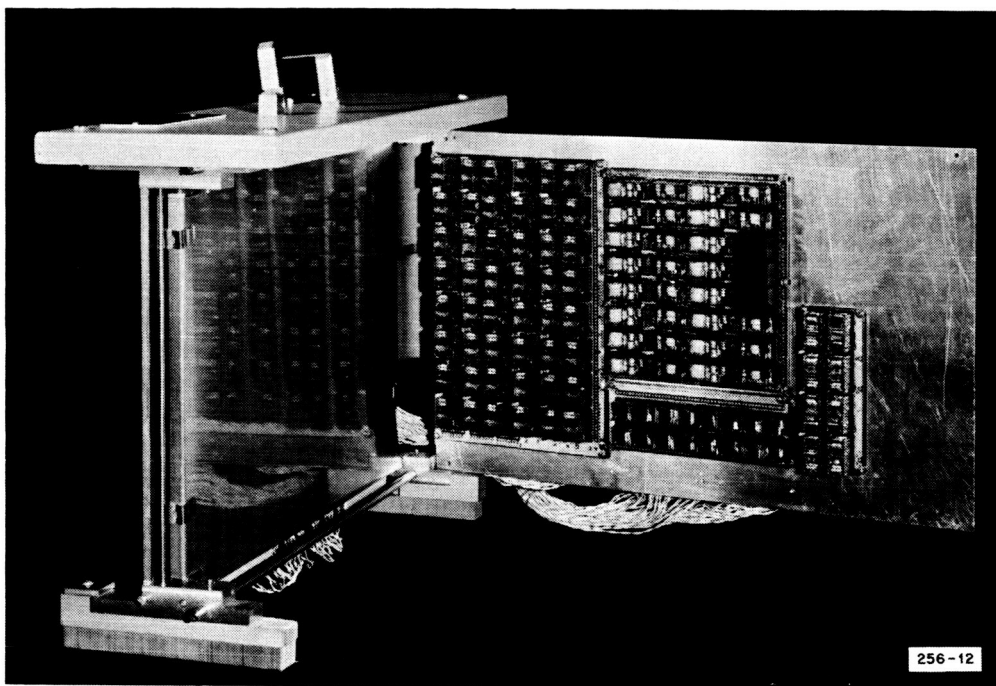
Figure 57. View Showing Bit-Sense Matrix and Sense Amplifiers
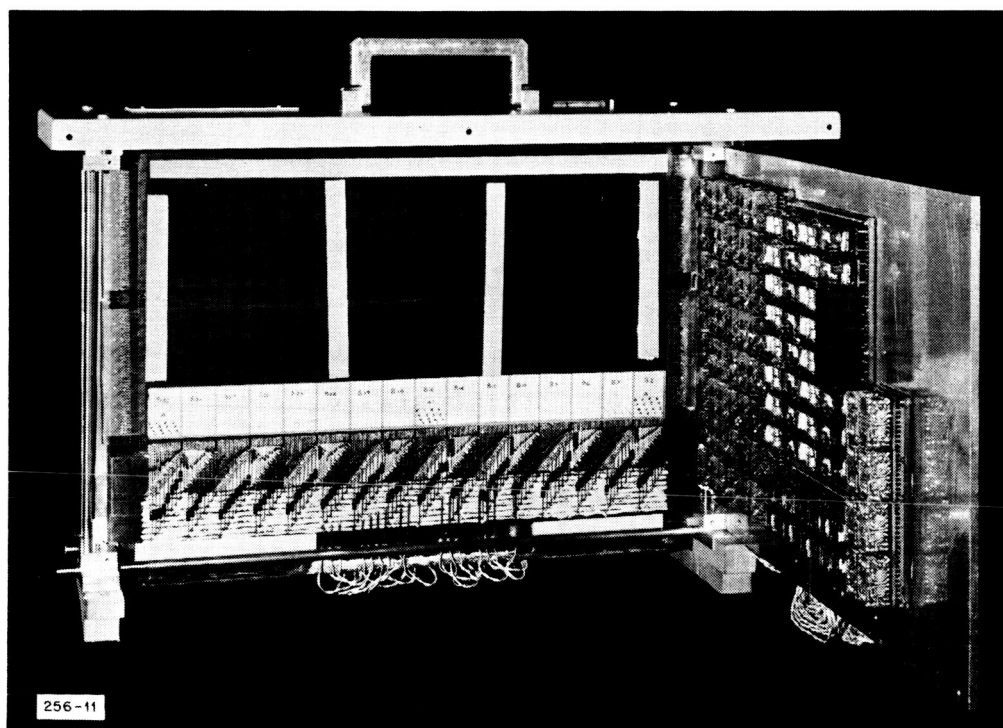
Figure 58. View Showing One Side of the 100,000-Bit
Memory Plane

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The final selection depended upon the use of a wire-formed male contact and a metal female sleeve. The sleeve was soldered into a multilayer backboard to allow insertion and removal of the modules. The wire-formed male contacts were cast in place as an integral part of the header. The female sleeve was later eliminated in favor of direct insertion into plated-through holes in the backboard.

Internal interconnection of components within the modules was accomplished by soldering to redundant printed-wiring boards for low-usage modules and by point-to-point welding for higher-usage modules. The ruggedness of both types of assemblies was adequately demonstrated during design and testing of the system. In order to make the modules more resistant to damage caused by changes in temperature and humidity, they were coated with polyamide-epoxy resin after final assembly. During temperature cycling tests several intermittents developed in the backboard-to-circuit-module connections; these were eliminated by soldering all the modules directly into the backboard.

4.2. MEMORY PLANE

The memory plane substrate was constructed of aluminum honeycomb with copper facing on both sides. Spacers of lightweight epoxy were used in areas where insulated feed-throughs were required.

The word-line solenoids were constructed of copper-clad glass-epoxy laminate with embossed epoxy grooves for positioning of the plated wires. Connections between the two memory planes on the surfaces of the substrate were accomplished with buss wire jumpers. Plated-wire connections around the edge of the plane were accomplished with etched copper-clad glass-epoxy transition jumpers. The word-line diodes were surface-soldered to the word lines and to the A-switch busses.

4.3. BACKBOARDS

The use of multilayered wiring was decided upon because of its compactness, its adaptability to controlled impedance interconnection, its ability to function as a mechanical support for the modules, and its adaptability for use in more condensed flight-model memories.

Several small multilayered backboards were used, and each of these backboards served a discrete functional part of the memory circuits. Use of small

sections, rather than one large board, provided for ease in making changes during design stages and for ease in fabrication involving the use of laboratory scale equipment. The multilayered boards are built up of copper-clad glass-epoxy laminate bonded together with B-stage preimpregnated glass-epoxy fabric.

The laminated thickness of all the sections is approximately 0.150 of an inch. Holes 0.035 of an inch were drilled at all required hole locations. Although solid carbide drills were used and care was exercised in selecting the proper speed and feed in drilling, there was evidence of resin contamination along the edges of the exposed copper on the internal layers. The resin was removed and all holes thoroughly cleaned by immersing and agitating in concentrated sulfuric acid for 15 to 45 seconds. A water rinse and a one-to-two minute dip in concentrated hydrofluoric acid were used to prepare the holes for electroless plating. As can be seen in Figure 60 the etching technique has not only cleaned away the unwanted epoxy drilling smear but has also undercut the glass epoxy at the internal copper interfaces so that a greater area for plated connection to the circuit layers is provided.

After electroless plating, the final electroplating is accomplished by the use of a phrophosphate copperplating bath. Use of the pyrophosphate bath has resulted in plated-through holes which meet the requirements of an internal diameter variation of 0.0295 to 0.037 of an inch without the need for extra reaming operations.

The multilayered backboard was designed to allow the use of Mylar artwork and to allow for circuit drilling without the need for precision machined drill jigs. This was accomplished by using 75-mil pads on 100-mil centers and by allowing no interconnecting circuitry to pass between any two adjacent pads. In all cases crossovers in layout were made on layers where the pad could be removed. This arrangement allowed for noncritical registration between layers.

Registration of artwork was accomplished by printing a master drilling pad pattern in register with a thin sheet of steel which had previously been drilled with a two-hole drill plate. Each successive layer of artwork was registered by alignment with the printed master drill pattern, by taping in place, and by drilling through the holes in the drill plate.
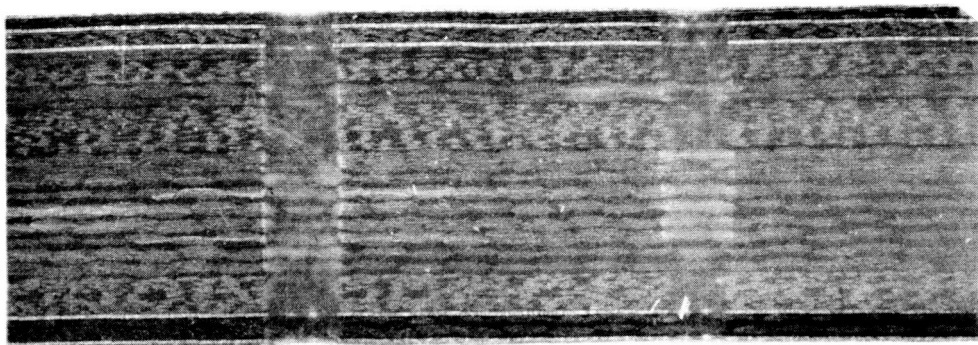
Chemically Treated Before Final Plating
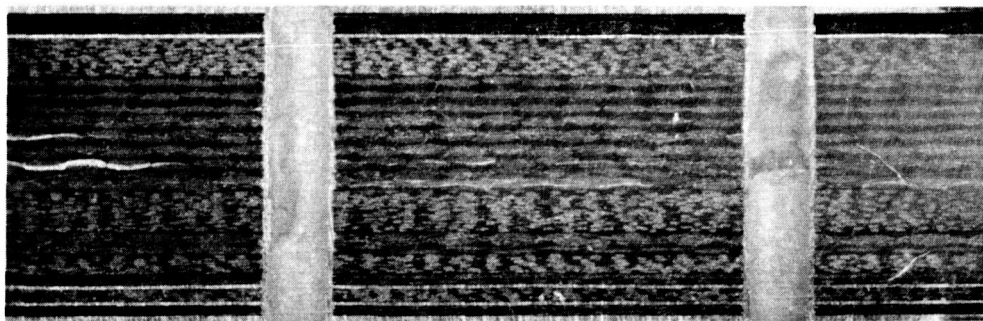
Finished Plated-Through Holes

Figure 59. Cross Section of Holes

A drill plate was made for each multilayered circuit board by printing and etching a pattern on 1/16-inch copper-clad glass epoxy. Each pattern was drilled by eye by using the etched-out center of the pads as locating means. With a little extra care in drilling at this stage it was found that sufficient accuracy would be obtained without the need for metal drill jigs.

4.4. INTERCONNECTIONS

Module interconnections were accomplished by use of multilayered backboards. Interconnections between the multilayered backboards and the plated wires and interconnections between the A and B busses on the plane and the multilayered backboard were made with flat-etched harnesses. The harnesses were attached to the multilayer with a connector using the same contacts used in the circuit modules.

During engineering design and testing several intermittent connections and open connections developed in the interconnecting harnesses; as a result, the harnesses were abandoned in favor of fine bi-filar wire soldered in place. Interconnections between sections and connections to the power connector were made with twisted pair wire.

4.5. CASEWORK

The memory plane was shielded with a gold flashed mu-metal shield coated with epoxy for electrical insulation. The backboards and memory planes were supported by an aluminum framework which was hinged to allow easy access to all parts of the memory. The entire structure was housed in an aluminum box measuring six inches by thirteen inches by twenty inches.

SECTION 5

MEMORY SYSTEM TEST RESULTS

5.1. ACCEPTANCE TEST

The following tests were performed at room temperature (25°C), at an elevated temperature (+50°C), and at a low temperature (-20°C). The total power input to the memory operating at a 100-kilocycle bit rate as a function of temperature is contained in Table 6. The d-c to d-c power converter was not temperature-cycled but was at room temperature throughout the test.

Table 6. Power Consumption for +28 Volt Input

Condition	-20°C (Watts)	+25°C (Watts)	+50°C (Watts)
100 Kilocycles Continuous Write	0.520	0.544	0.56
100 Kilocycles Continuous Read	0.420	0.436	0.443
Standby	0.190	0.189	0.195

In addition to the power consumption test, the memory was operated over the normal range of input voltage from +23 volts to +34 volts. The memory was tested with the abnormal input condition of +40 volts with repetitive one-millisecond transients of a peak amplitude of +70 volts. Although not required, the memory operated normally during these abnormal power supply conditions.

Various patterns of information were written into the memory at all temperatures. It was demonstrated that the storage of information in the memory was not affected by turning off the power and turning the power back on during continuous reading of the stored information.

It was demonstrated that the memory operated reliably at a bit rate in excess of the specified 100-kilocycle bits per second. Information errors occurred when the interval between clock pulses was eight microseconds.

5.2. OPERATING MARGINS TEST

During these tests the d-c to d-c converter was disconnected, and separate supplies were connected to the memory; as a result all the input voltages to the circuits were able to be varied. The +28 volt supply can be varied from +23.5 volts to +33.5 volts since it supplies a regulator and was not varied for the following tests once it was established that the regulator was functioning properly. The +12 volt, +5 volt, and -2.5 volt supplies were varied to determine the operating margins of the memory. The circuits were designed to operate with a ±2 percent variation in supply voltage, which is provided by the d-c to d-c converter.

At room temperature (+25°C), the memory system functions with no errors with a variation in supply voltages of ±10 percent. With a voltage variation exceeding ±10 percent several types of errors may occur. With high-input voltages, the sense amplifier gain may be so high as to trigger on noise, while at low-input voltage conditions, the sense amplifier may fail to trigger an input that would normally trigger it.

At the extreme temperatures of +50°C and -20°C, the memory will operate without errors with a variation in supply voltages of ±10 percent with a normal information pattern (approximately one half of the 16-bit channels being stored as 1's and the other half being stored as 0's.) With the worst-case pattern (one bit different from the other 15-bit channels), the memory will tolerate a ±5 percent variation in the supply voltages. Since the system will operate with supply voltages of ±2 percent, a reasonable margin exists. A plot showing the operating area of the plated-wire array as a function of the drive currents is shown in Figure 60.

The worst-case pattern discussed above is not a function of the plated-wire array but of the circuits. Crosstalk between the 16-bit channels exists in the bit-sense matrix as well as in the wiring. This crosstalk limits the allowable voltage variation when one bit is different from the other 15 bits since the crosstalk to the one bit out of phase is maximum under these conditions.
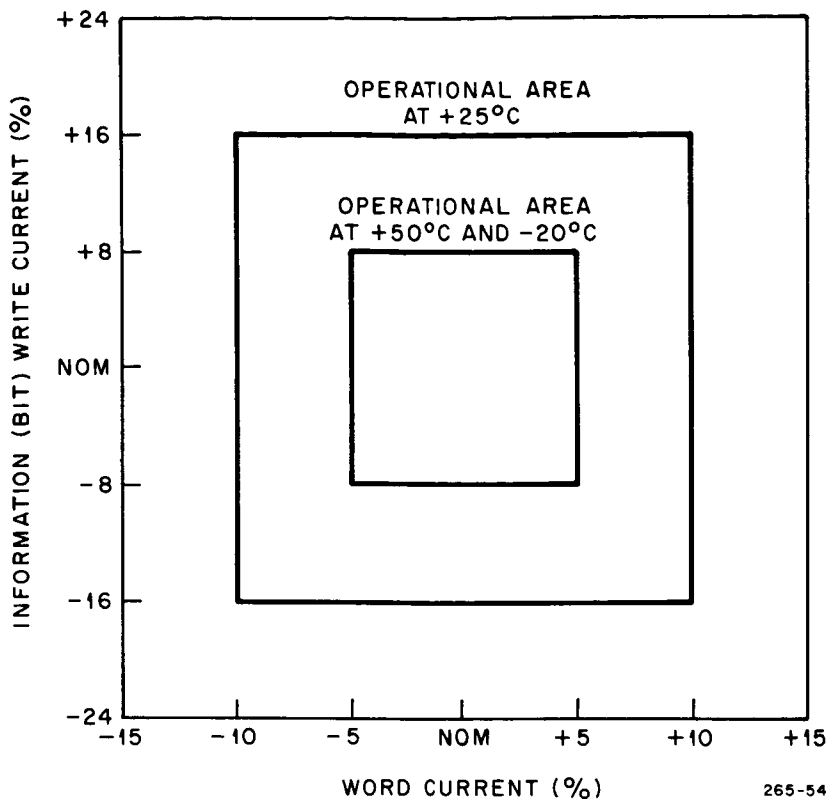
Figure 60. Graph Showing Boundary of Operating
Region of Plated-Wire Memory Array at Which One or
Two Errors are Made for All Operating Temperatures

An intermittent error was observed while the memory was being heated
from room temperature. This error did not recur but during the interval be-
tween the hot test and the cold test, inspection revealed a fractured etched-
circuit conductor which was repaired before proceeding. This etched-circuit
wiring harness, which connects the memory plane to the bit-sense matrix has
since been replaced. In addition, the circuit modules have been soldered in
place to make a more reliable connection to the backboards.

SECTION 6

CONCLUSIONS AND RECOMMENDATIONS

6.1. PRESENT AND POTENTIAL OPERATING CHARACTERISTICS

A reliable, low-power, thin-film spacecraft memory has been designed, fabricated, and successfully operated over a temperature range of from -20°C to $+50^\circ$C. The memory utilizes plated wires for the storage element and contains 98,304 bits which can be accessed bit serially at any bit rate up to 100,000 bits per second. The memory has a maximum power dissipation of 0.560 watt.

Since 16 bits are written into or read out of the memory in parallel, internally the memory proper is driven at a rate of 6.25 kilocycles when the system is operating at 100 kilocycles. With a plated-wire switching time of approximately 100 nanoseconds, it is obvious that the memory elements are driven at an extremely low duty cycle. Furthermore, it is apparent that the serial bit rate can be greatly increased with only a reorganization of the system and an increase in power.

The circuitry is packaged in cordwood modules which are arranged to facilitate testing and to provide test points necessary for complete performance evaluation. Using packaging techniques suitable for a flight model, considerable reduction in size and weight can be achieved. Table 7 summarizes projections based on the present achievements. The use of integrated circuits would reduce the volume required to package the circuits, however, this probably would result in an increase in power at the present state-of-the-art.

In summary, the memory met or exceeded all specifications with the exception of the power supply which had been subcontracted to a vendor who was not willing or able to fulfill his contract.

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Table 7. Projected Memory Operating Parameters

Type of Memory	Capacity	Information Bit Rate	Power Dissipation (Watts)	Volume (Cubic Inches)	Weight (Pounds)
Buffer	100,000	100 kilocycles	0.32	140	4
	1,000,000	100 kilocycles	0.60	420	15
	2,800,000	500 kilocycles	1.20	624	45
Random-Access	8192 words of 10 bits each	10-kilocycle word rate with 5 micro-second access time	0.4	140	4
	8192 words of 20 bits each	1-megacycle word rate with 0.4-microsecond access time	20	350	10

APPENDIX I

Appendix I contains the memory logic diagrams.
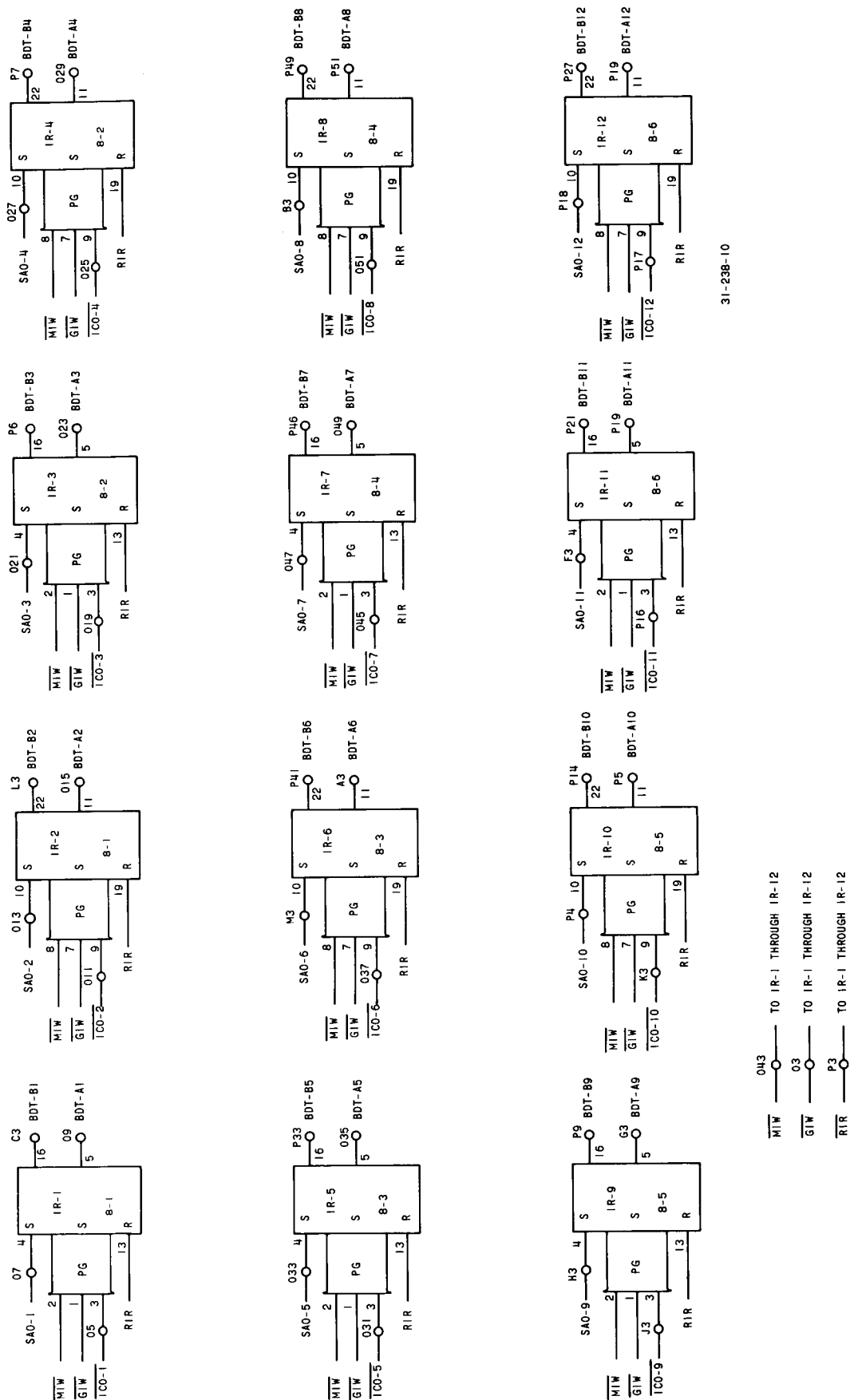
Figure I-1. Information Path, Logic Diagram (Part 1 of 2)

31-238-10

Figure I-1. Information Path, Logic Diagram (Part 2 of 2)

Figure I-2. Sense Amplifiers and Bit Drivers, Logic Diagram
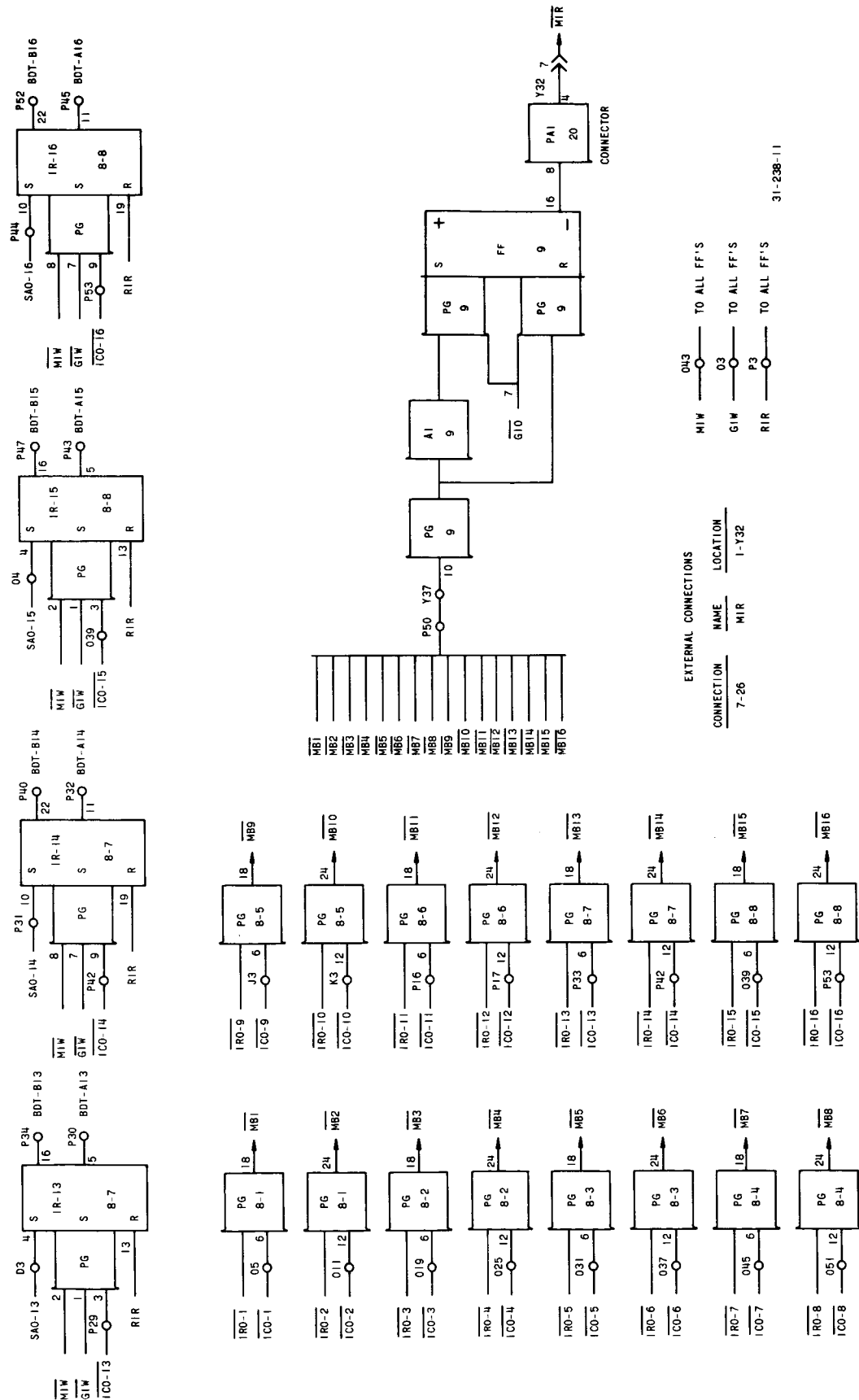
Figure I-3. Information Ring Counter, Logic Diagram
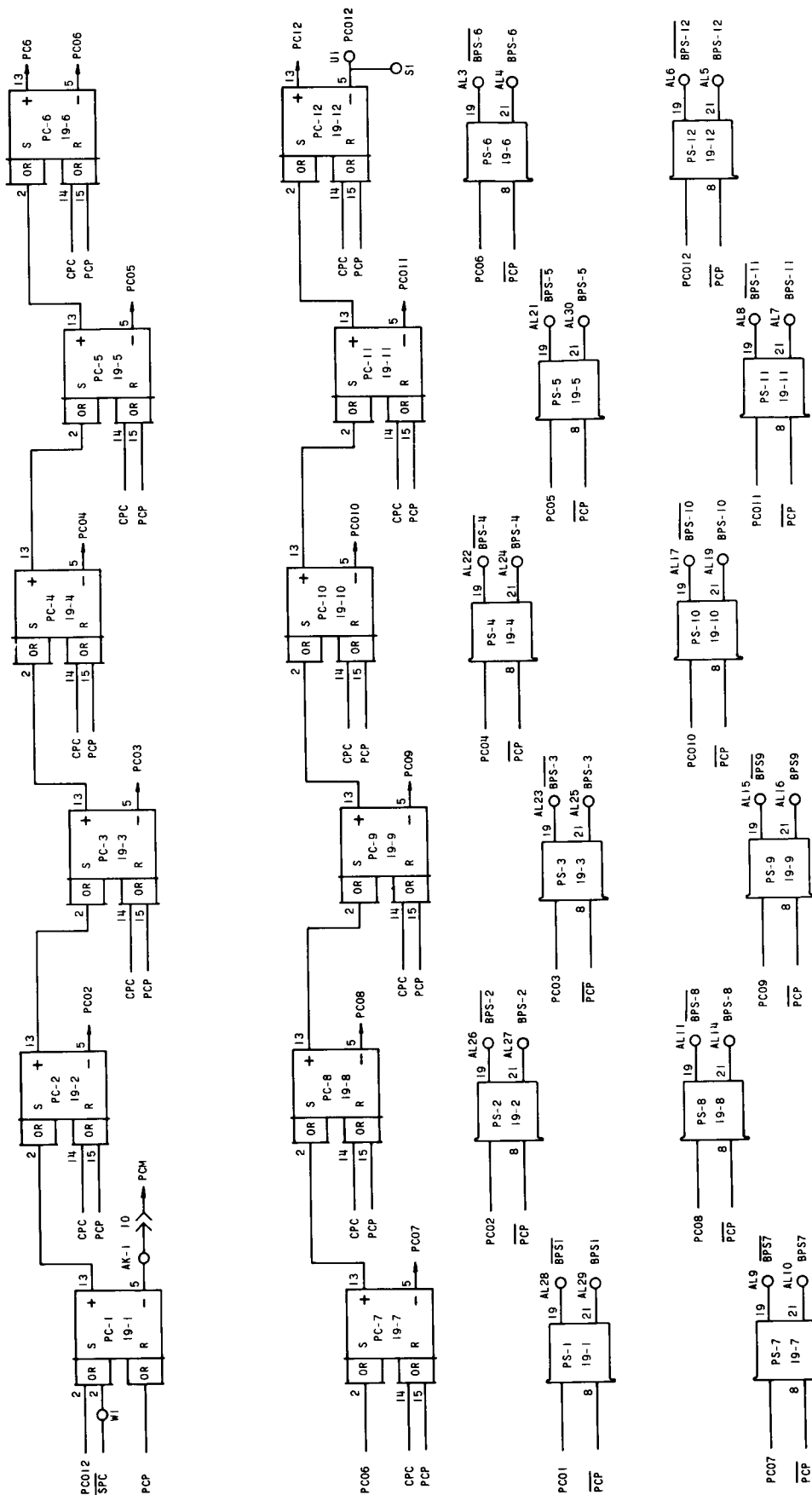
Figure I-4. Bit-Position Counters and Drivers, Logic Diagram
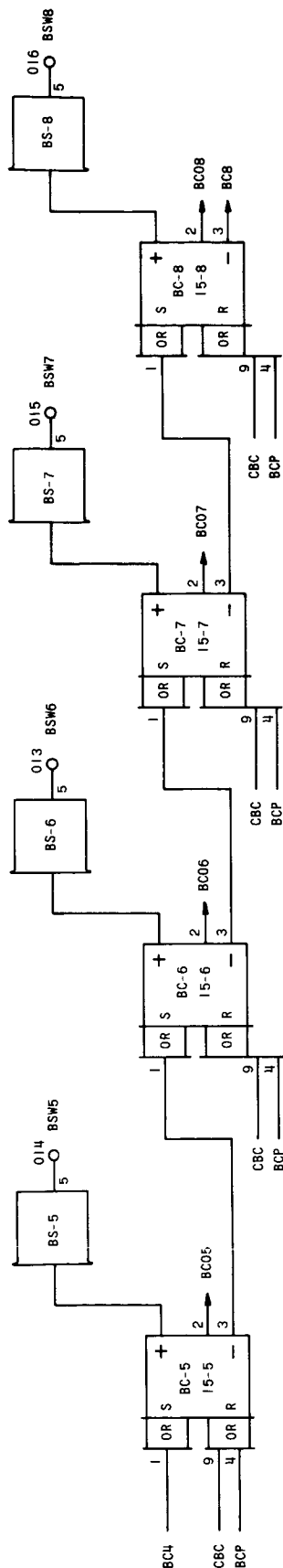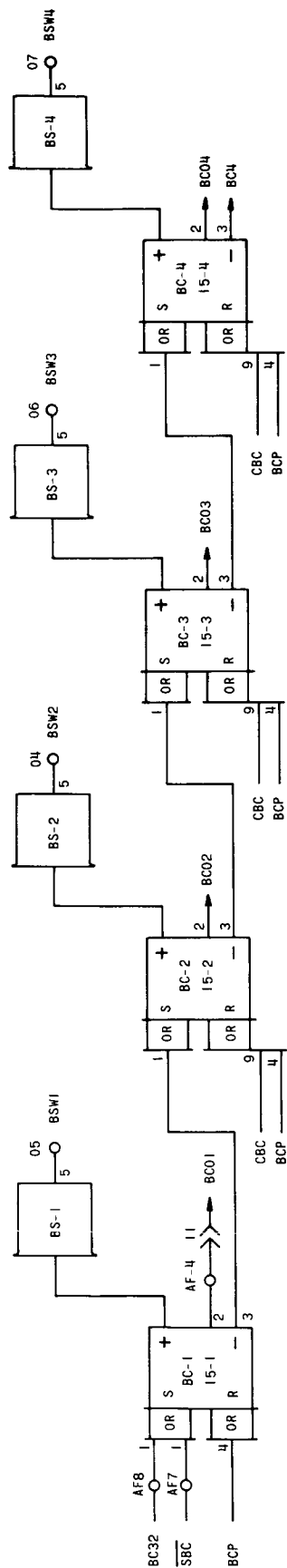
31-238-16

EXTERNAL CONNECTIONS

CONNECTOR	NAME	LOCATION
10-29	PCM	19-AK1

Figure I-5. B-Counters and Switches, Logic Diagram (Part 1 of 4)
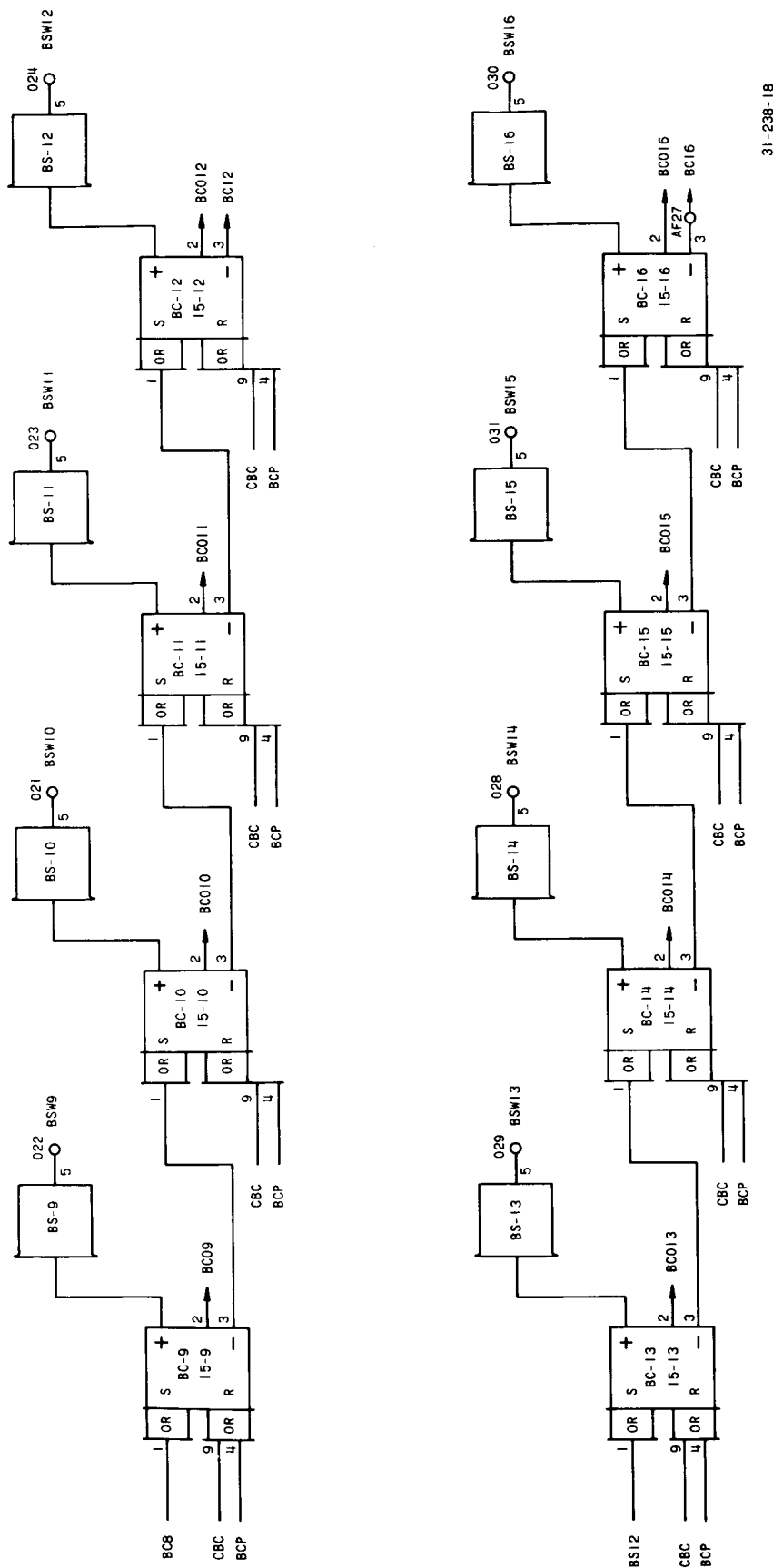
31-238-17

Figure I-5 B-Counters and Switches, Logic Diagram (Part 2 of 4)
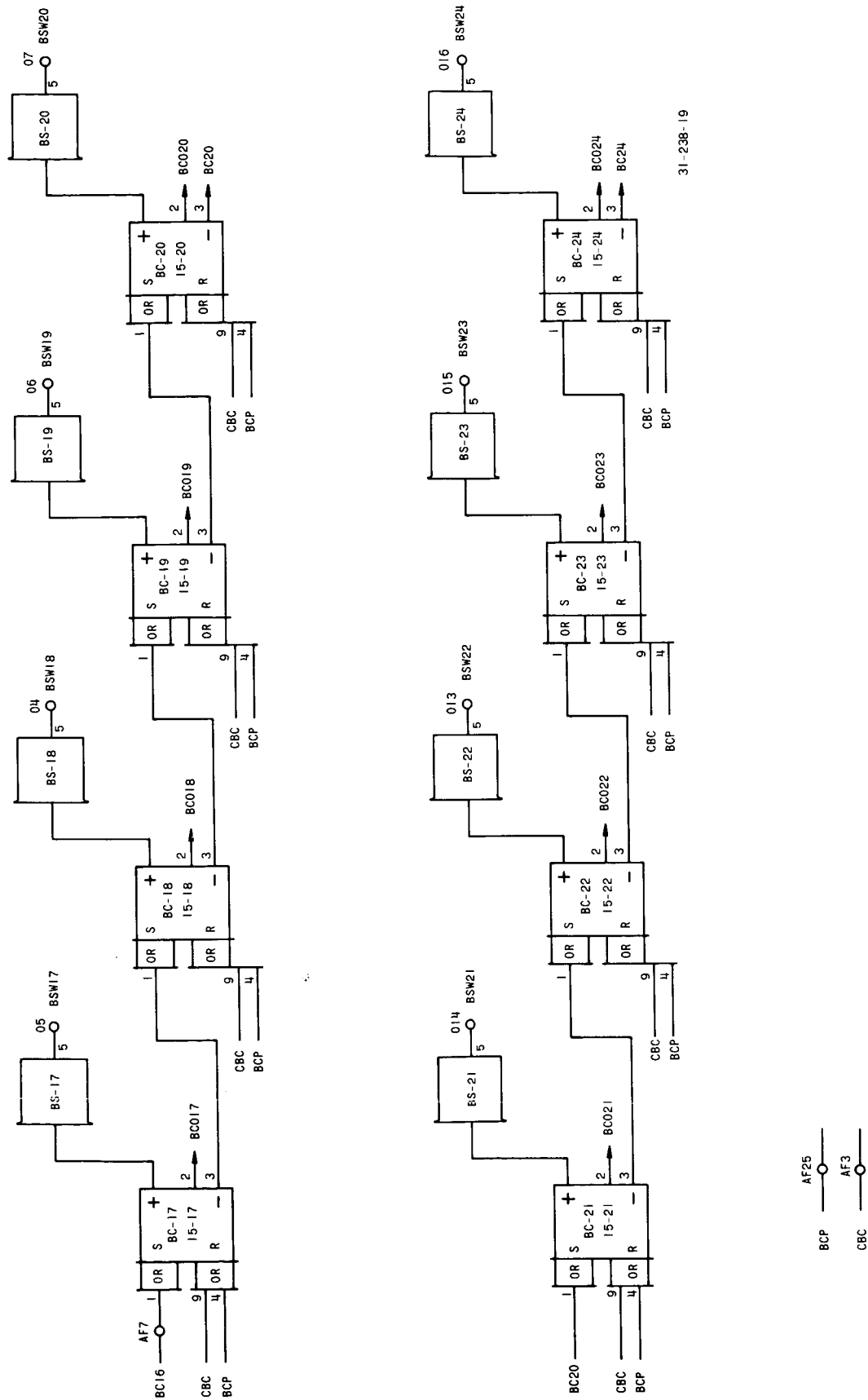
Figure I-5. B-Counters and Switches, Logic Diagram (Part 3 of 4)

31-238-19
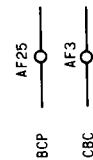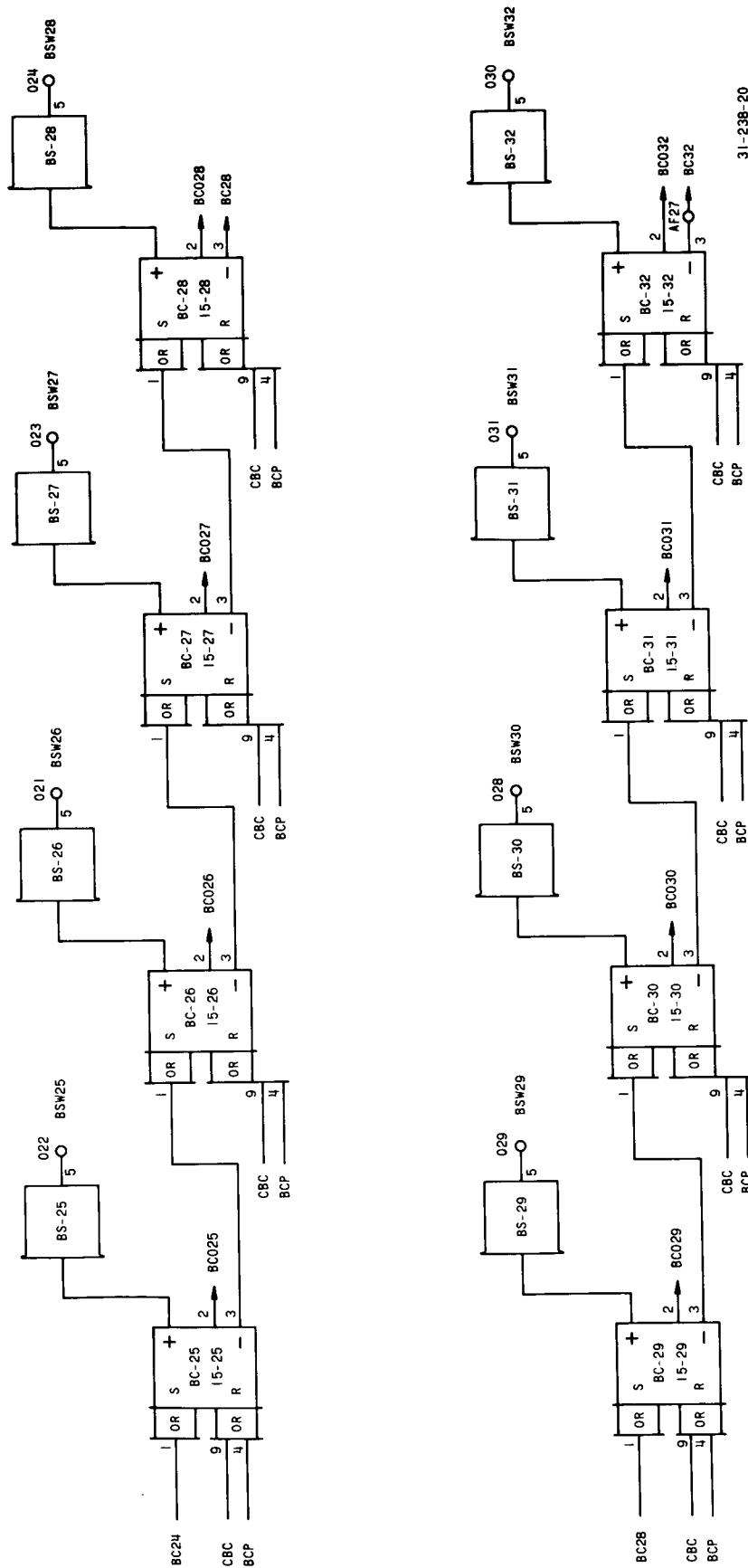
Figure I-5. B-Counters and Switches, Logic Diagram (Part 4 of 4)

Figure I-6. A-Counters and Switches, Logic Diagram (Part 1 of 2)
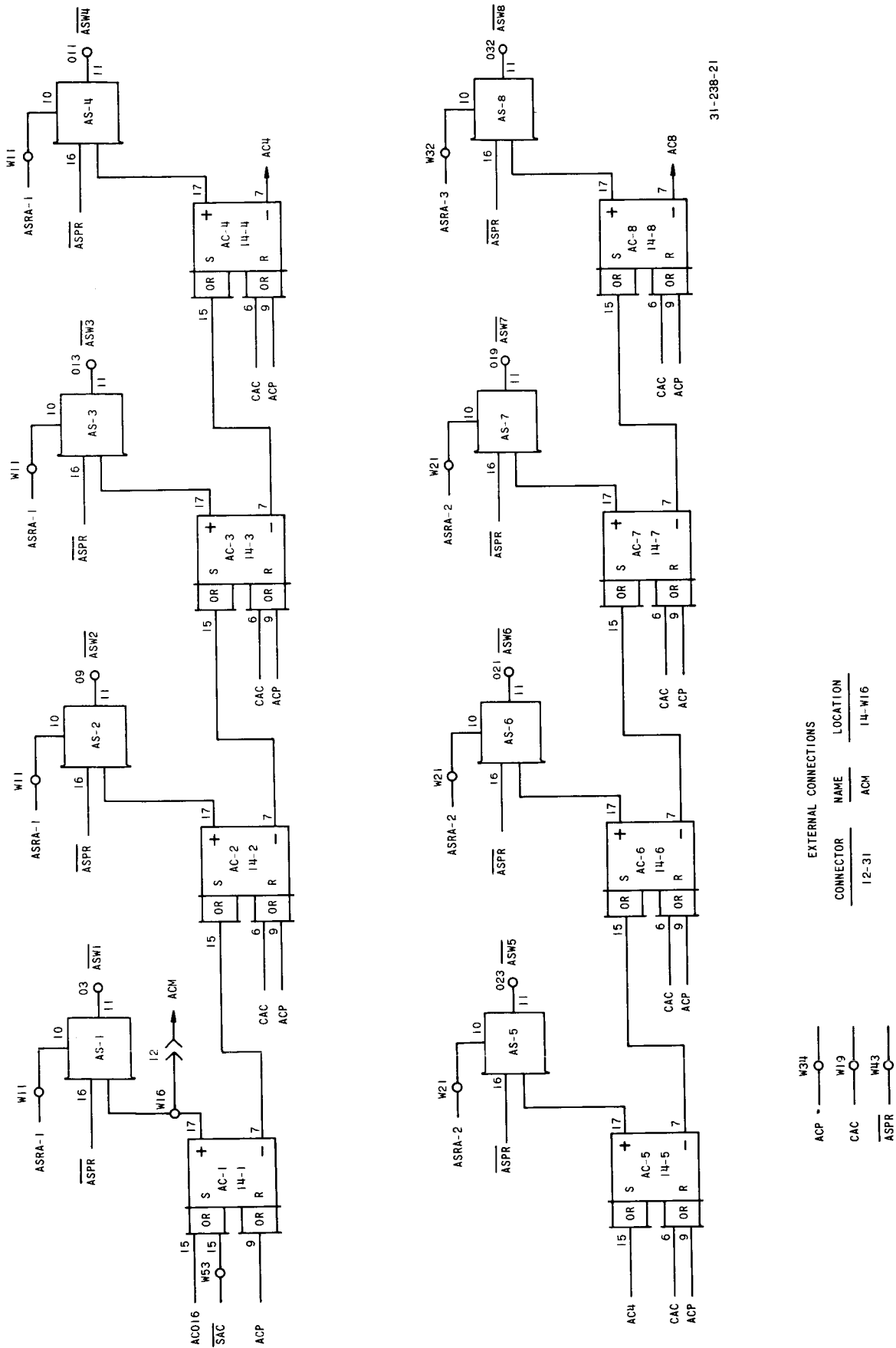
31-238-21
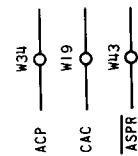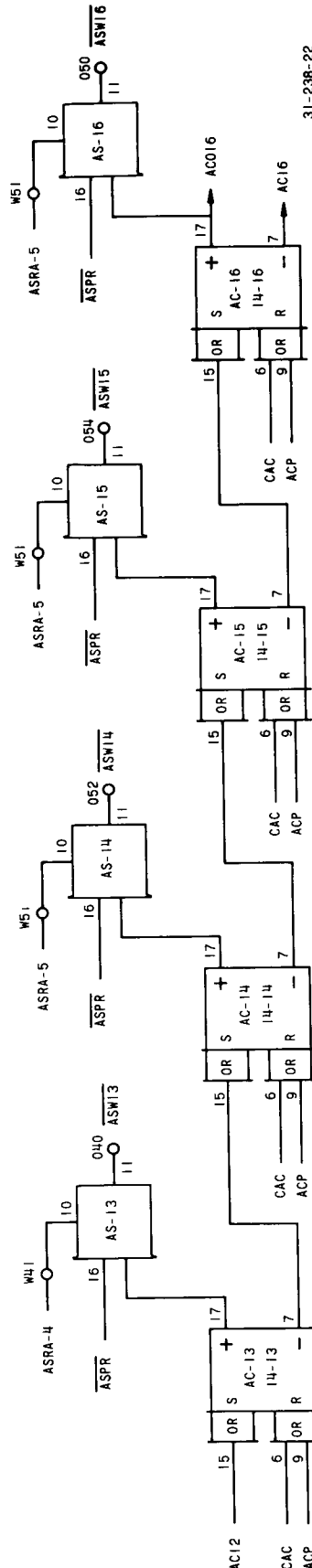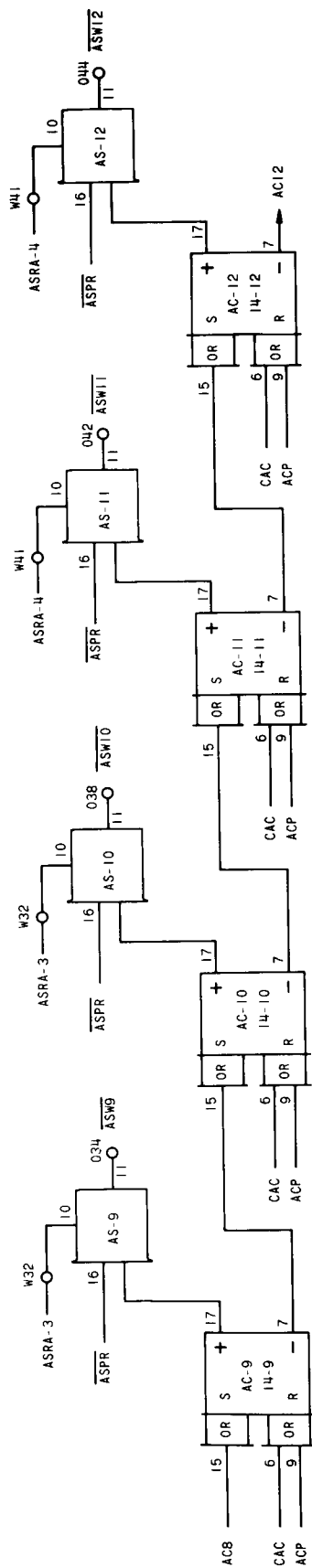
Figure I-6. A-Counters and Switches, Logic Diagram (Part 2 of 2)

31-238-22

Figure I-7. Timing and Control, Logic Diagram

31-238-23

I-13
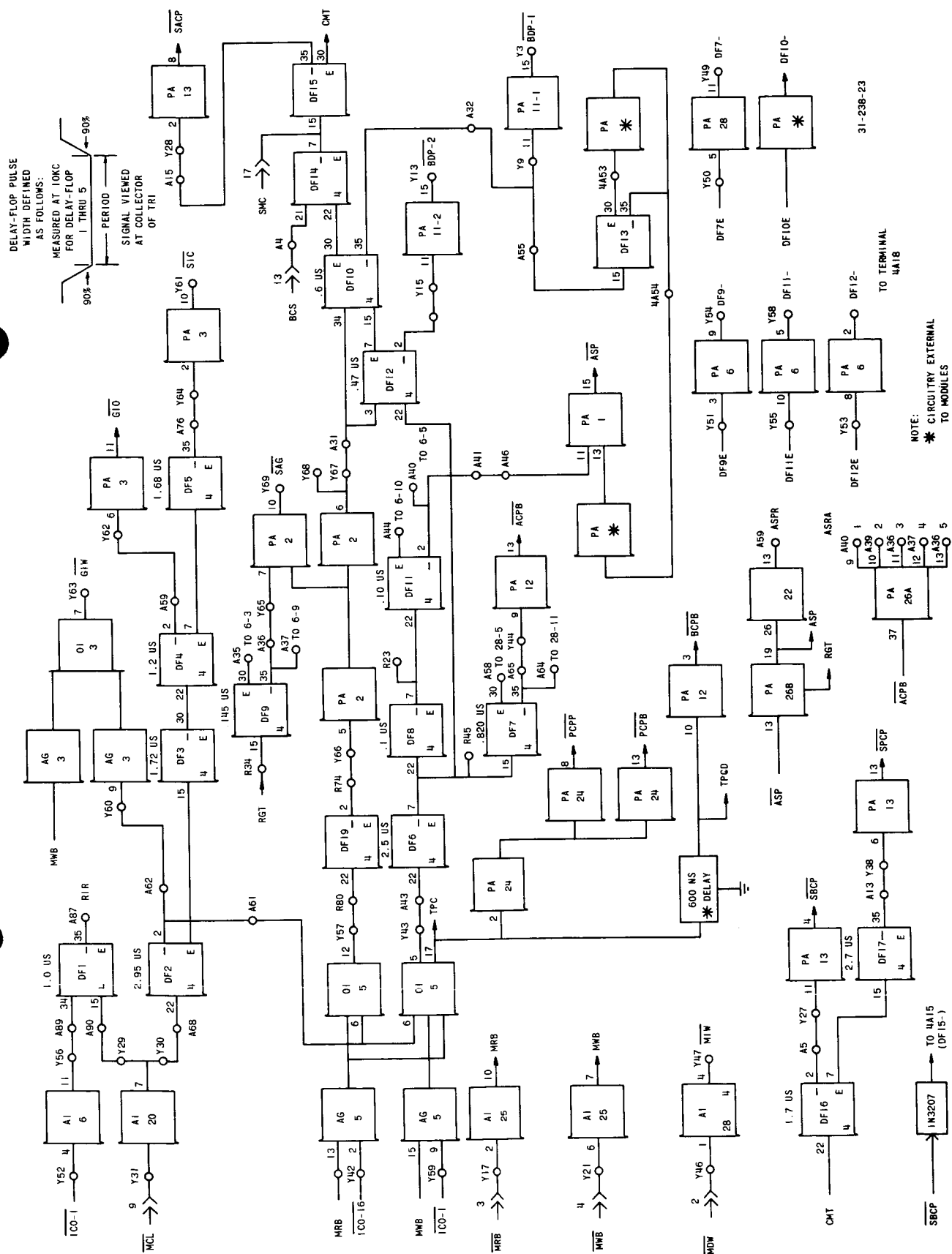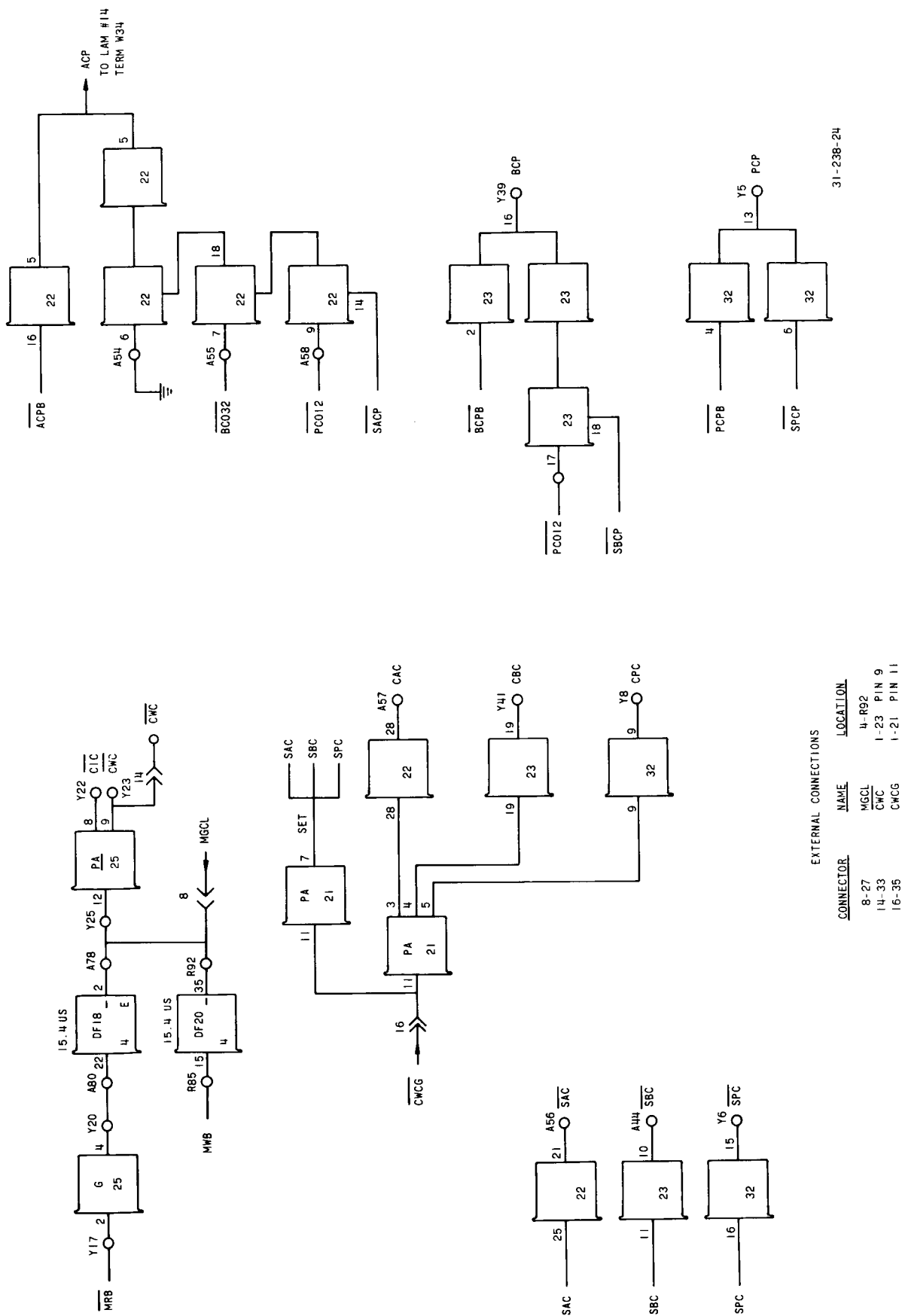
Figure I-8. Counter Controls, Logic Diagram

Figure I-9. Plated-Wire Selection Data

Figure I-10. Bit-Sense Matrix Selection, Logic Diagram

APPENDIX II

Appendix II contains schematic diagrams and parts lists of the modules used in the memory.

NOTES:
ALL DIODES TYPE 1N3207.
ALL RESISTANCE VALUES ARE
IN OHMS.
ALL CAPACITANCE VALUES ARE
IN PICOFARADS.
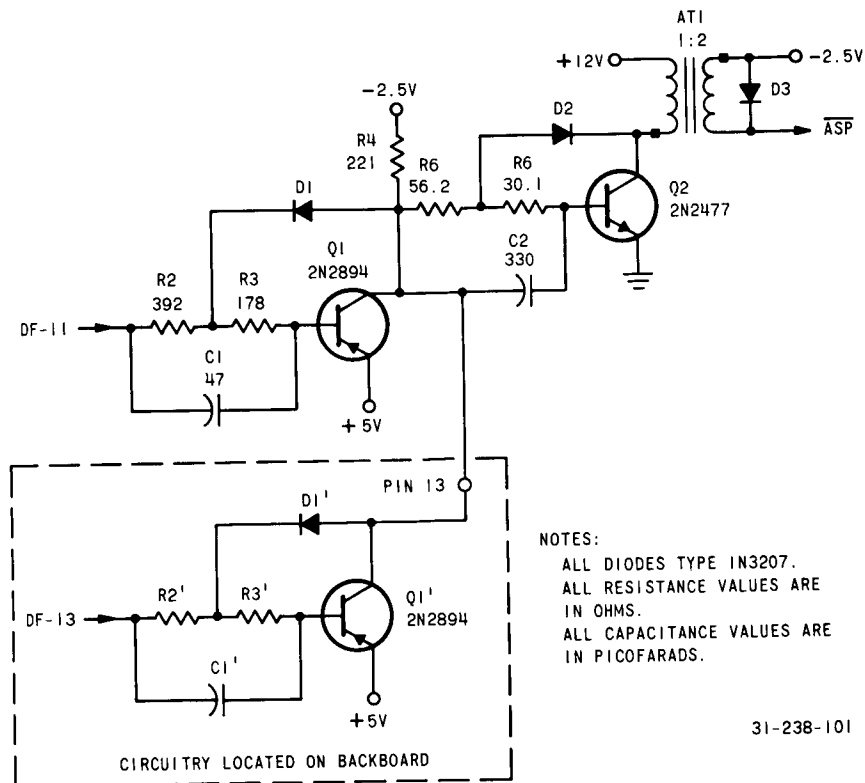
31-238-101

Figure II-1.   A-Switch Driver

NOTES:
RESISTANCE IS IN OHMS UNLESS
OTHERWISE SHOWN.
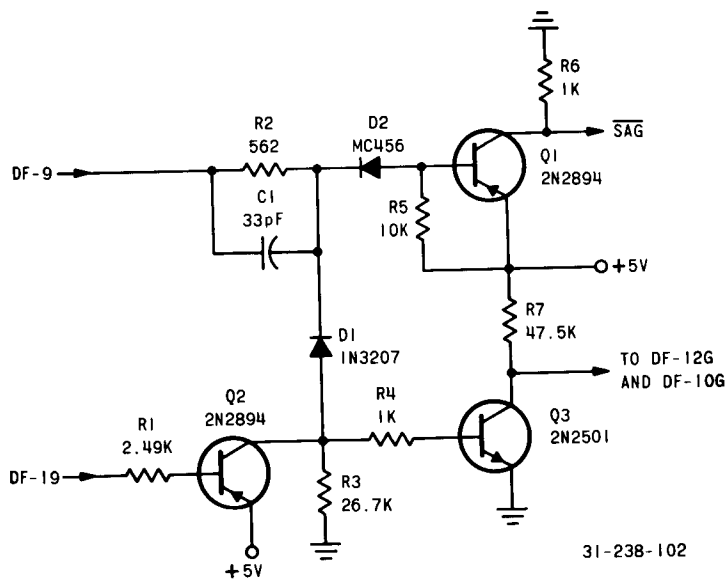
31-238-102

Figure II-2.   Sense Amplifier and Bit
Driver Trigger Circuit

II-2
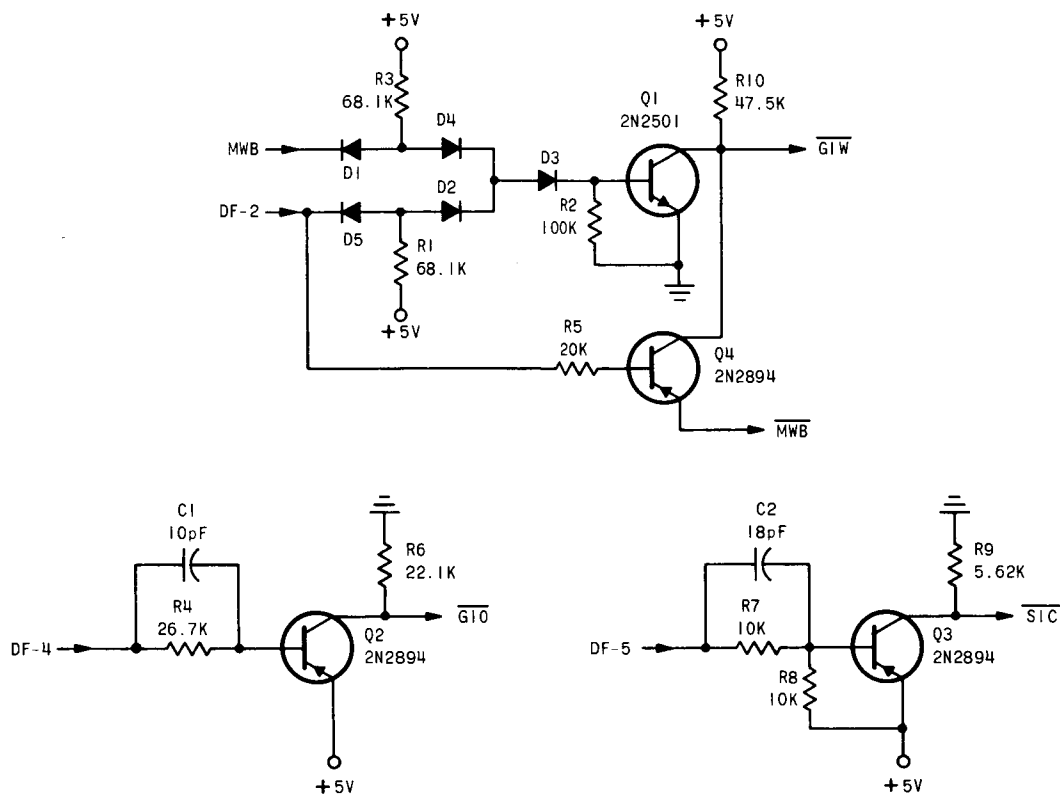
NOTES:
DIODES (D1,2,5) TYPE 1N3207
(D3,4) TYPE MC456

31-238-103

Figure II-3. Gate In/Out Circuits and Information Register
Counter Step Circuit
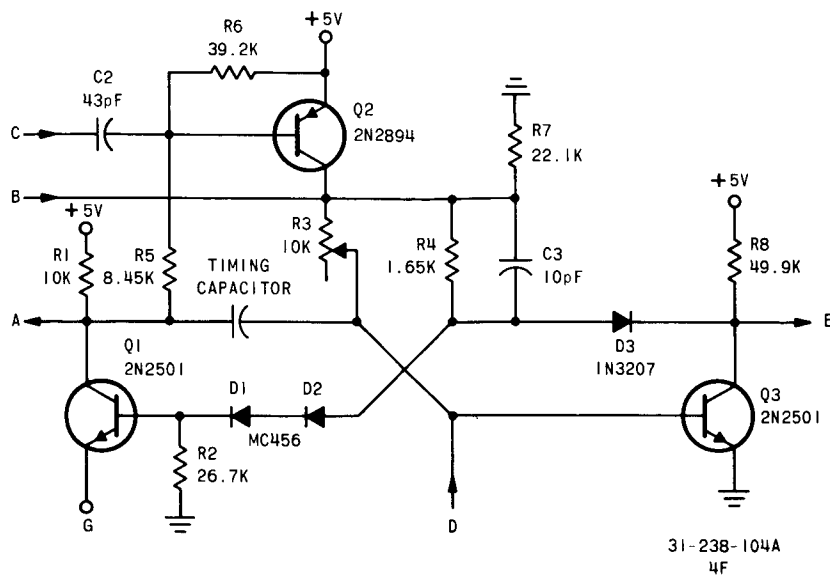
Figure II-4. Delay-Flop
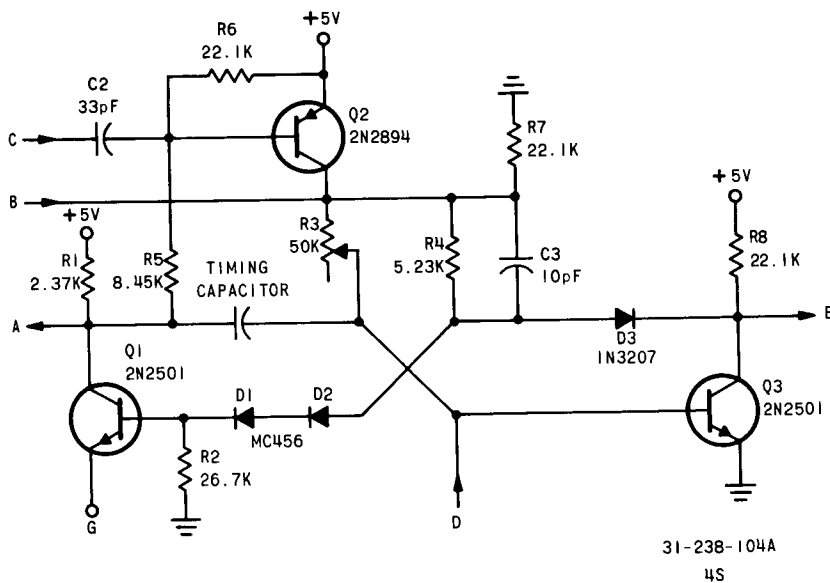
Figure II-5. Delay-Flop
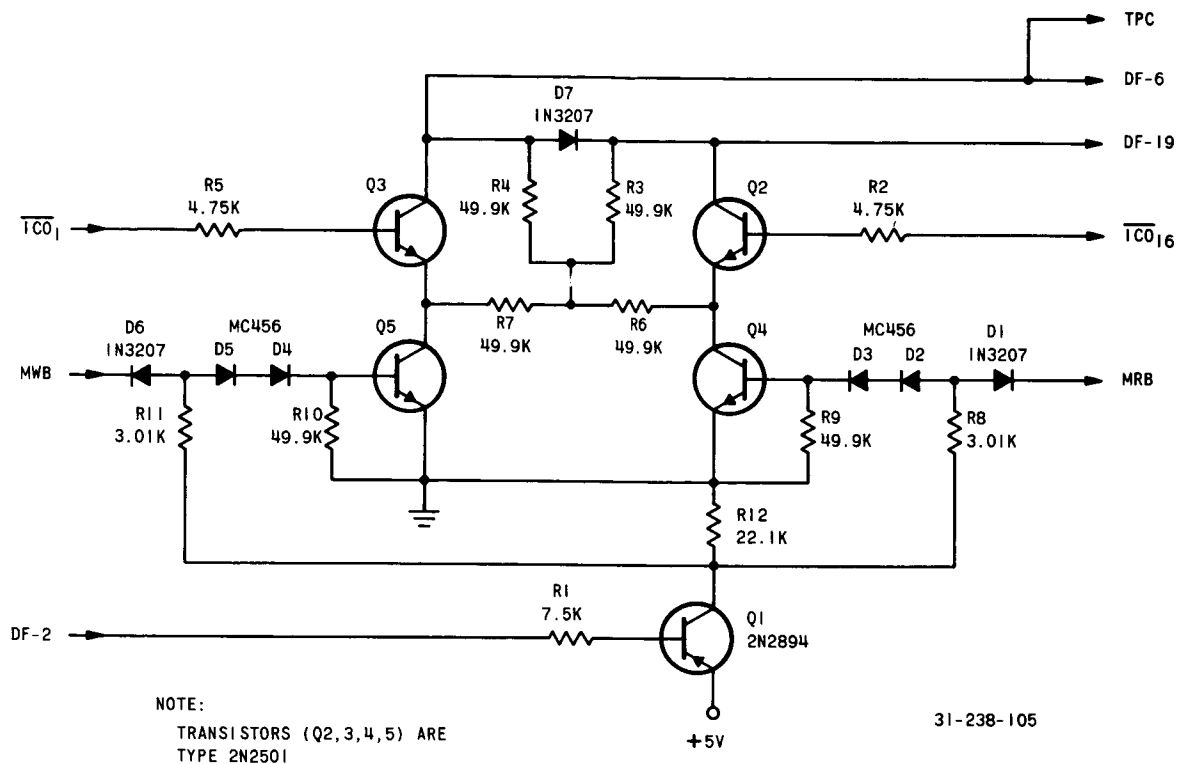
Figure II-6. Read/Write Trigger Gate
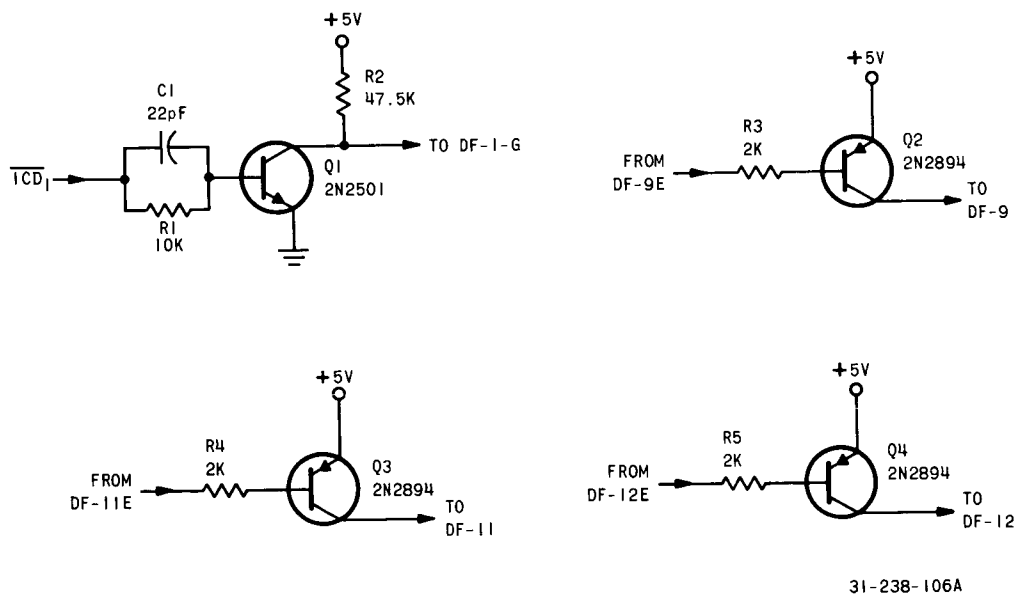
Figure II-7. Delay-Flop Discharge Circuits

NOTE:
DIODES (D1,2,3,4,5,7,8,9,12,13,14,16) ARE
TYPE IN3207. ALL OTHERS TYPE MC456.
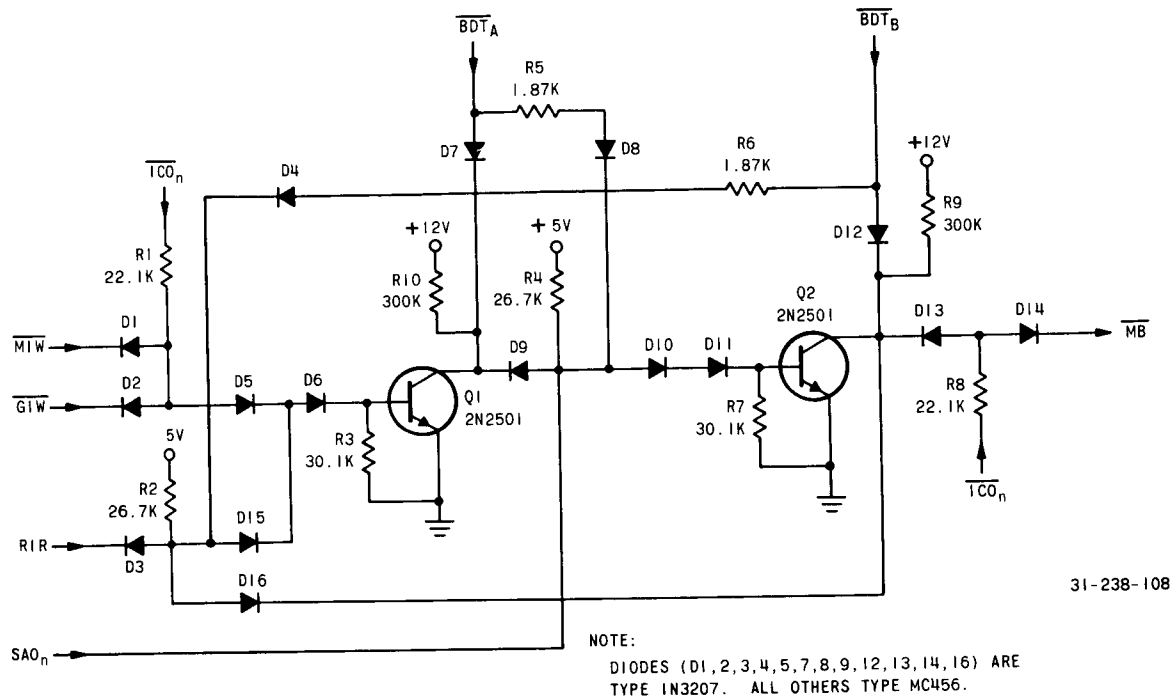
31-238-108

Figure II-8.   Information Register

NOTE:
ALL TRANSISTORS TYPE 2N2501
DIODES (D1,3,4,9,10,12,14) TYPE MC456
DIODES (D2,5,6,7,8,11,13) TYPE IN3207
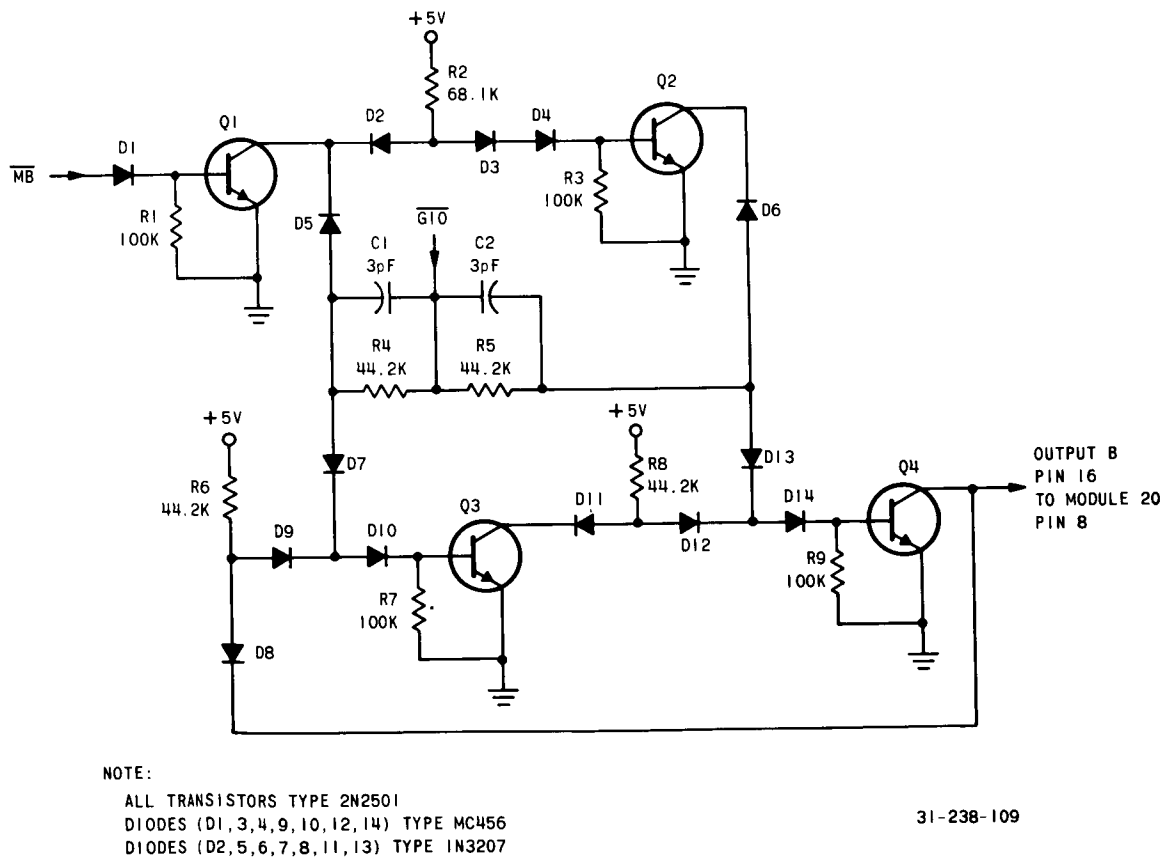
31-238-109

Figure II-9.   Information Buffer
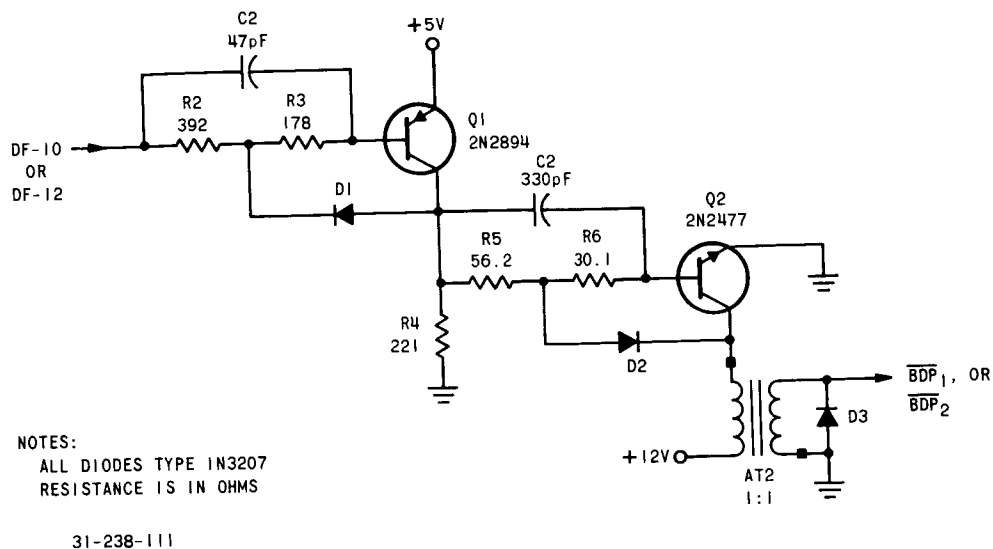
Figure II-10. Bit-Driver Pulse
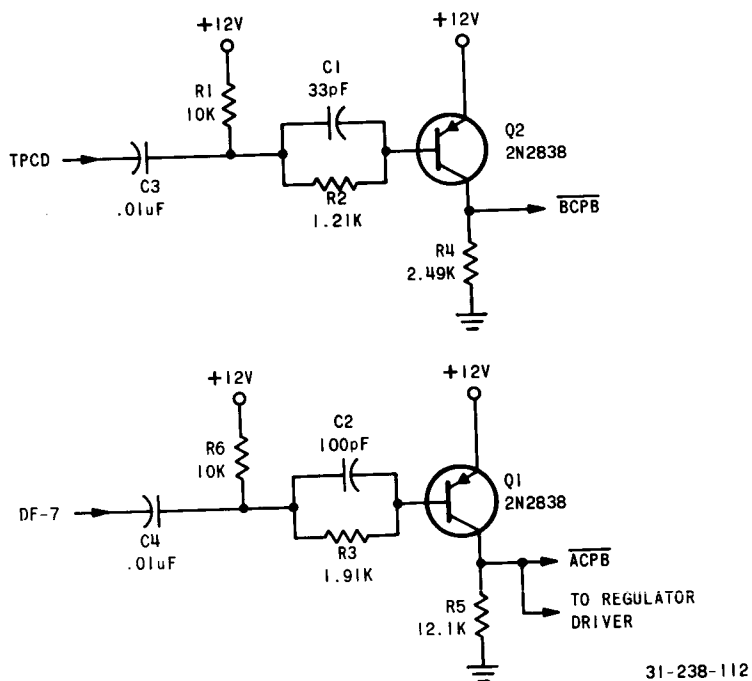
Figure II-11. A and B-Counter Drivers
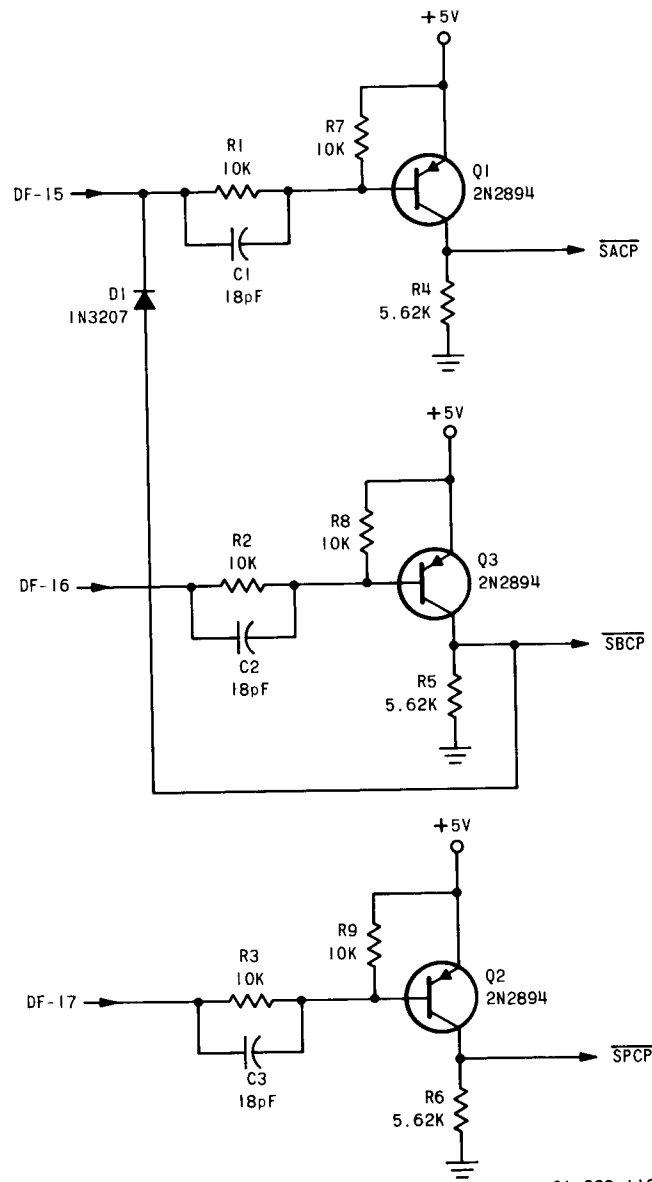
Figure II-12.   A,B and P-Counter
Stepping Circuits
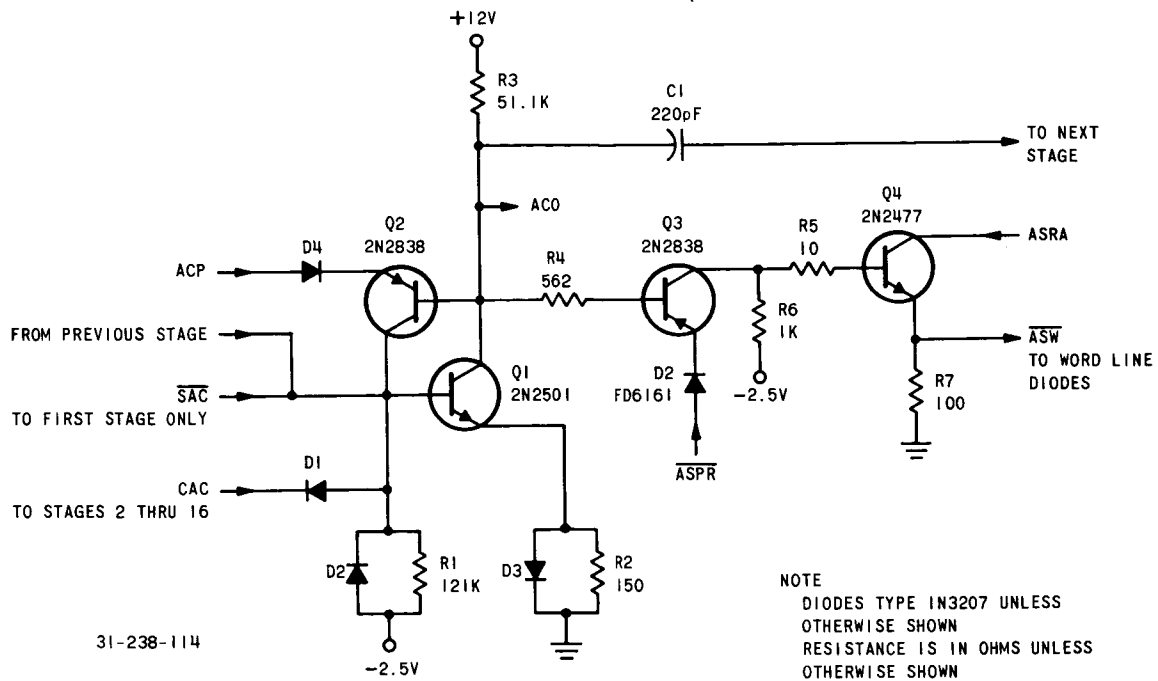
Figure II-13. A-Switch and Counter
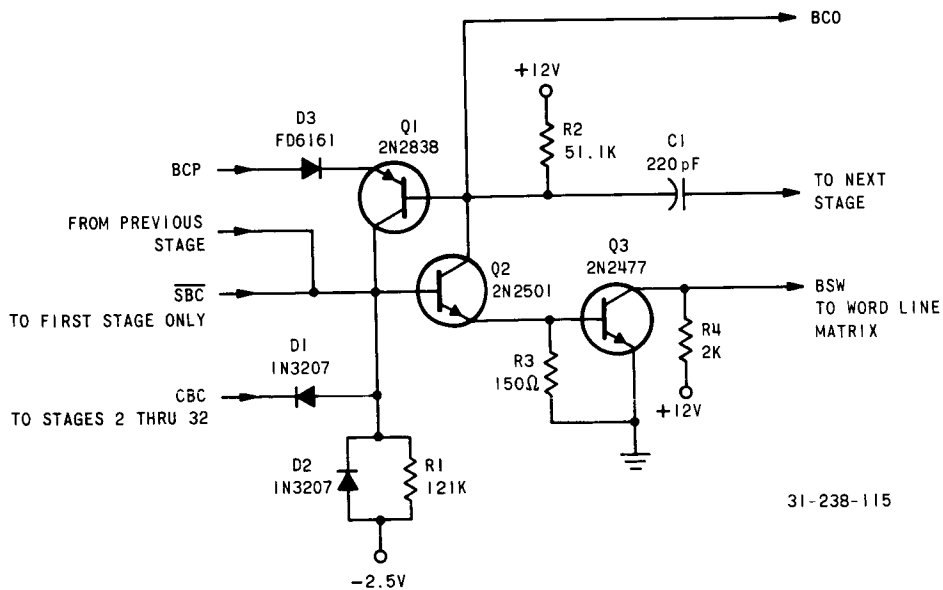
Figure II-14. B-Switch and Counter

II-9

NOTE:
TRANSISTORS (Q13,5,7) ARE TYPE 2N2501
TRANSISTORS (Q2,4,6,8) ARE TYPE 2N995

31-238-116

Figure II-15. Bit-Sense Matrix

NOTE:
RESISTANCE IS IN OHMS UNLESS
OTHERWISE SHOWN
ALL DIODES TYPE 1N3207

31-238-117A

Figure II-16. Read Amplifier
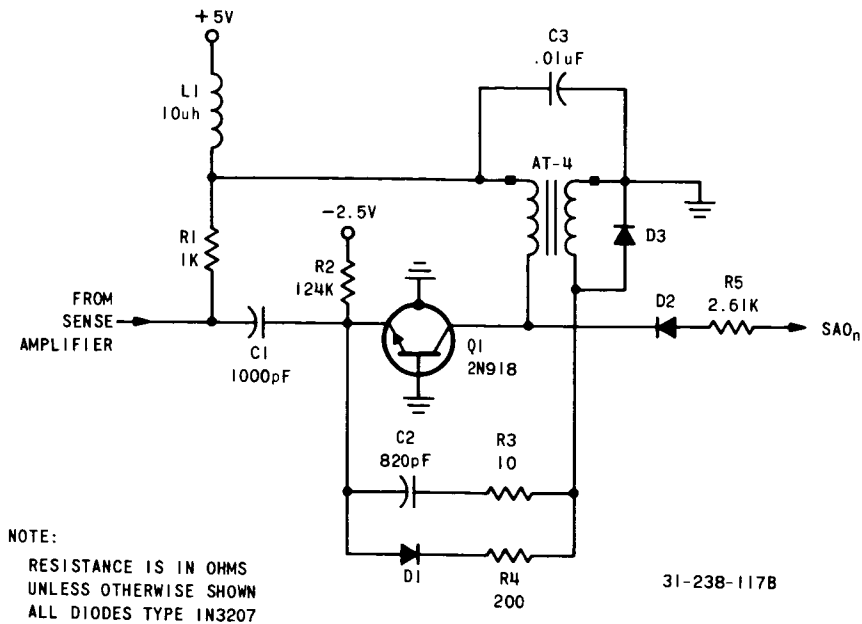
Figure II-17. Blocking Oscillator
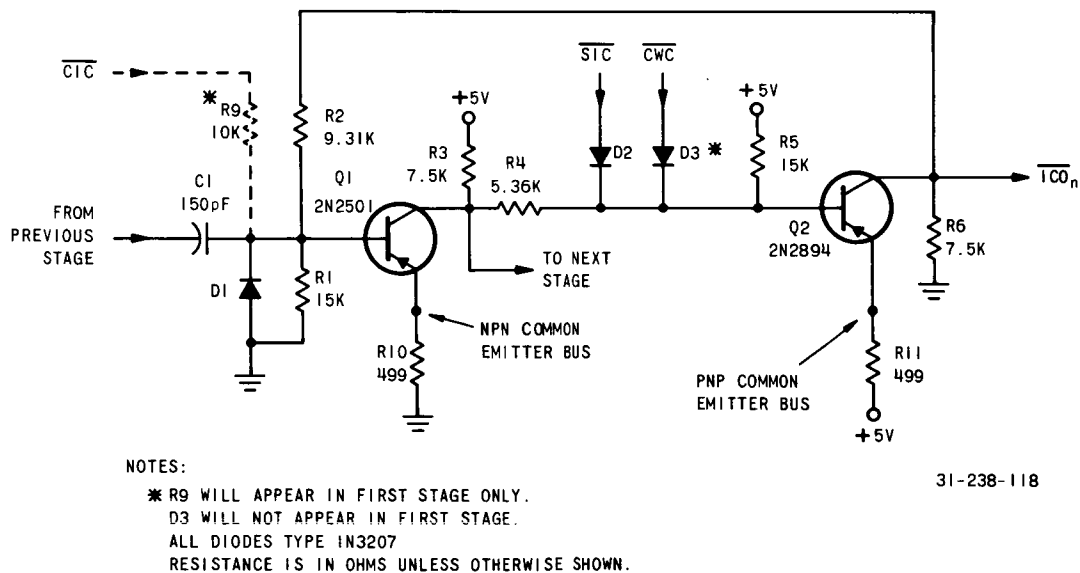
Figure II-18. Information Ring Counter
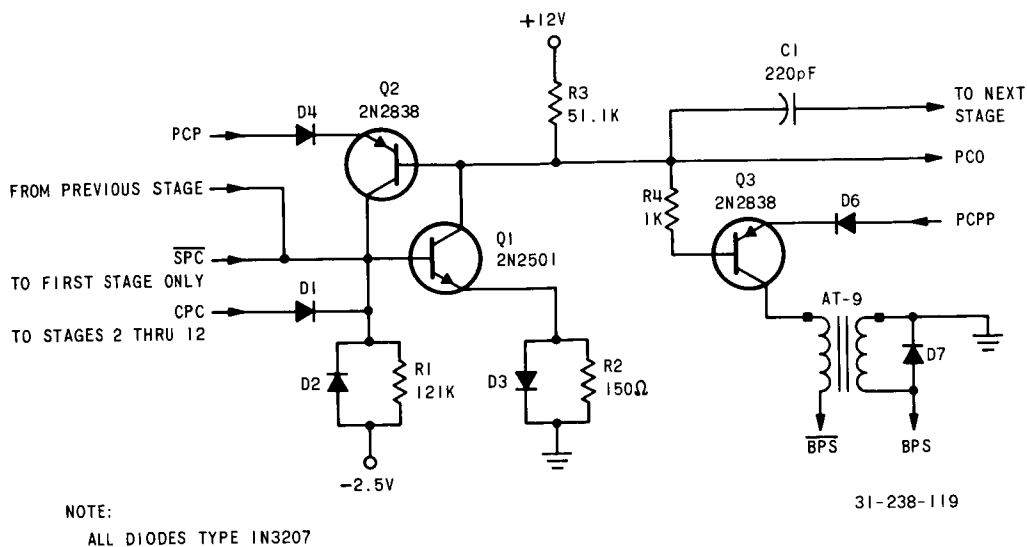
Figure II-19. Bit-Position Counter and Drive Circuit
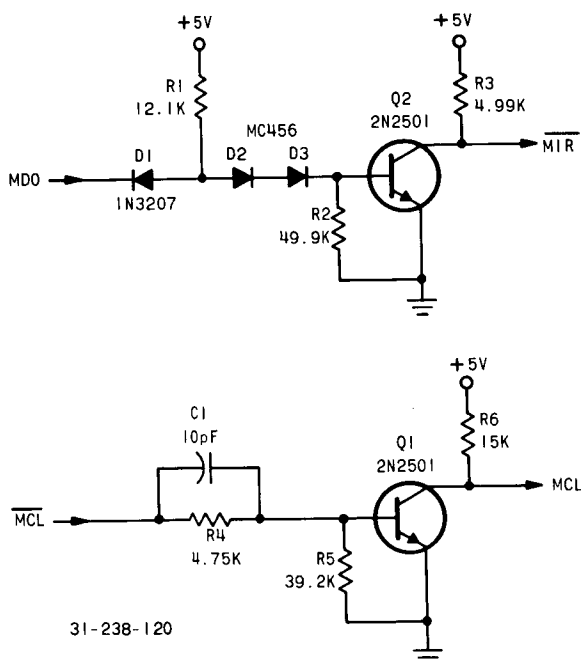
Figure II-20. Memory Clock
Amplifier and Output
Information Driver
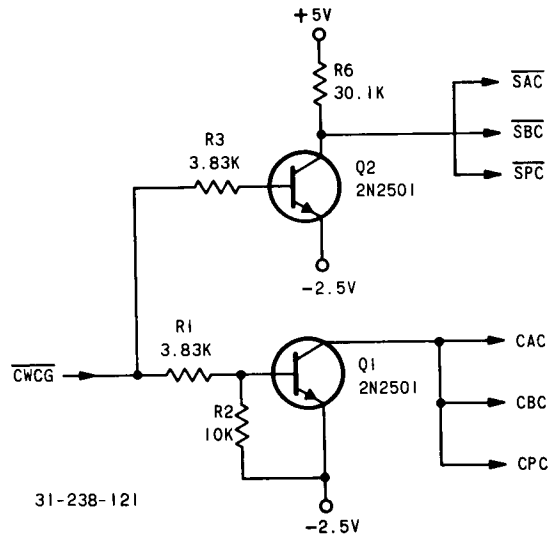
Figure II-21. Counter Clear
and Set Circuits

Figure II-22. A-Counter Gate
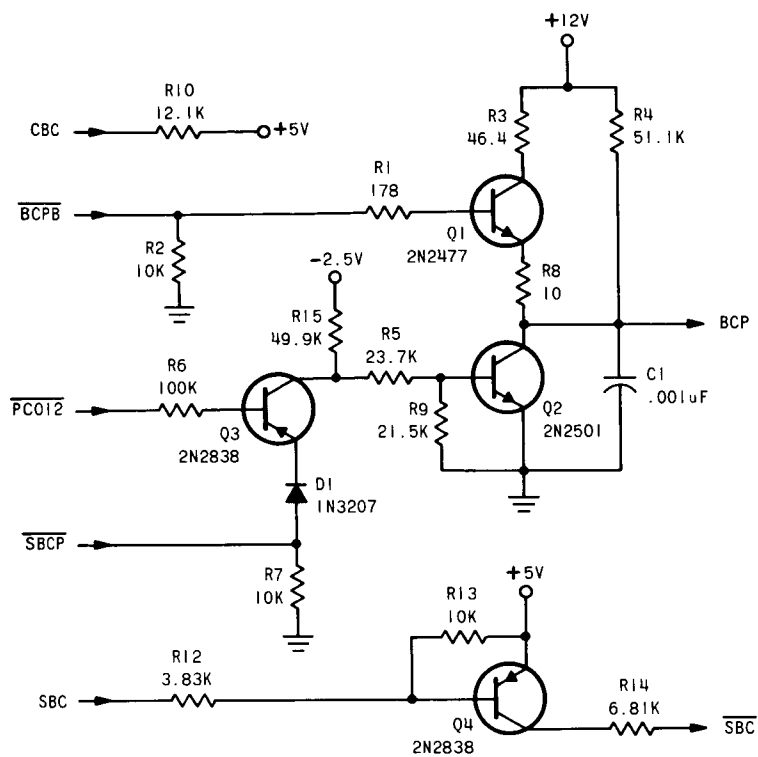
Figure II-23.   B-Counter Gate
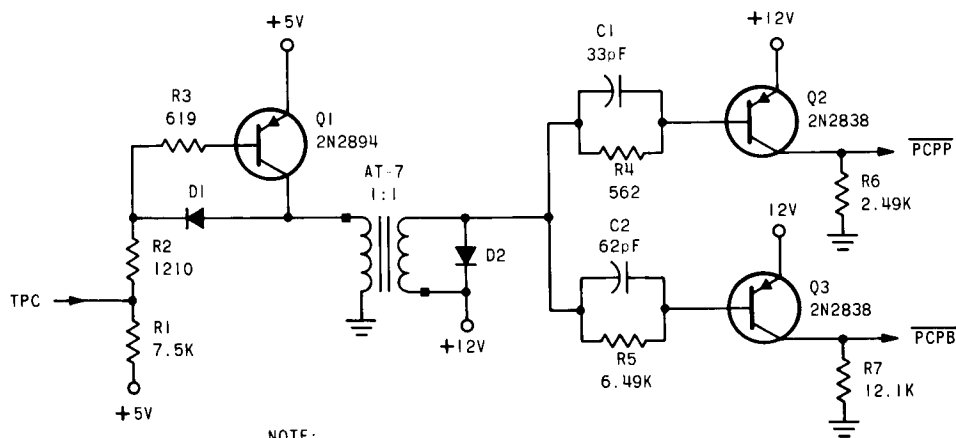
Figure II-24.   Position-Counter Driver

Figure II-25. Input Preamplifier and
Clear Pulse Generator
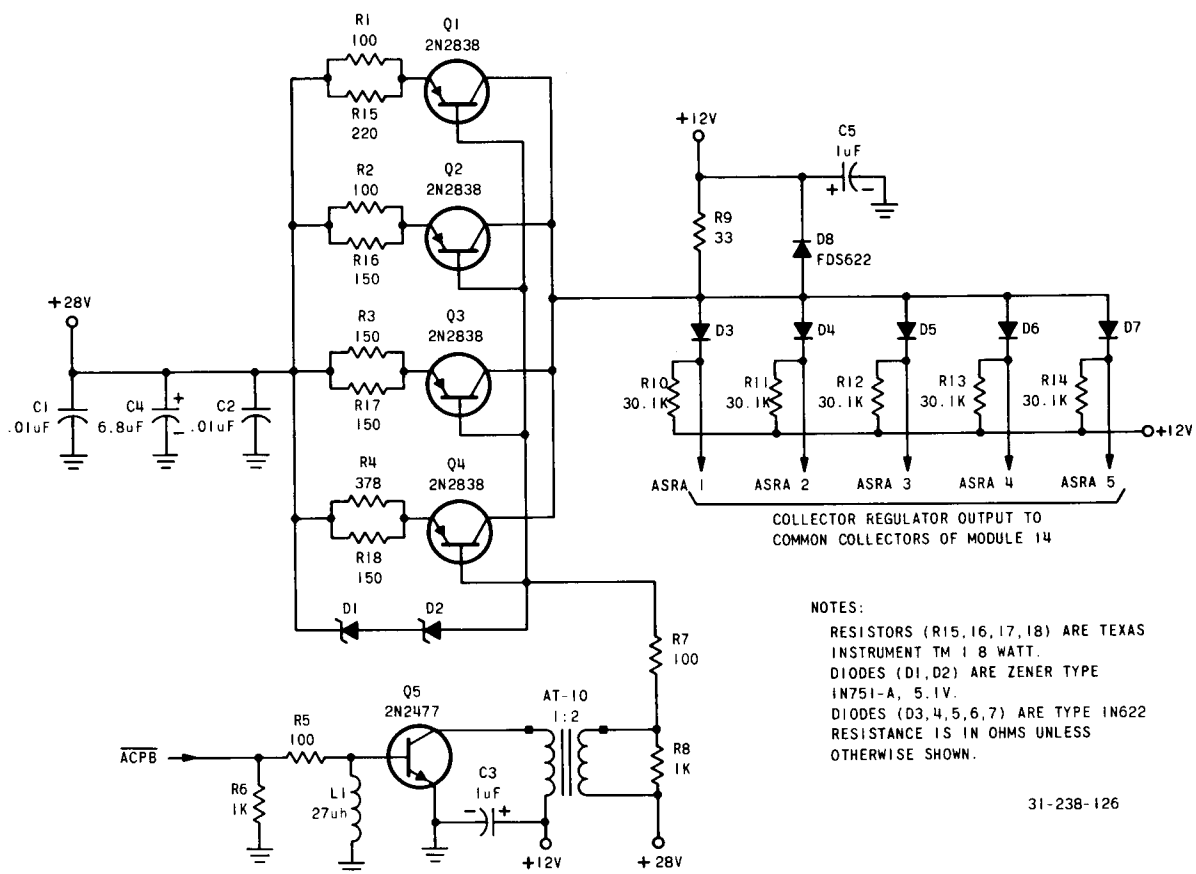
Figure II-26. Word-Current Collector Regulator

NOTES:
RESISTORS (R15,16,17,18) ARE TEXAS
INSTRUMENT TM I 8 WATT.
DIODES (DI,D2) ARE ZENER TYPE
IN751-A, 5.1V.
DIODES (D3,4,5,6,7) ARE TYPE IN622
RESISTANCE IS IN OHMS UNLESS
OTHERWISE SHOWN.

31-238-126
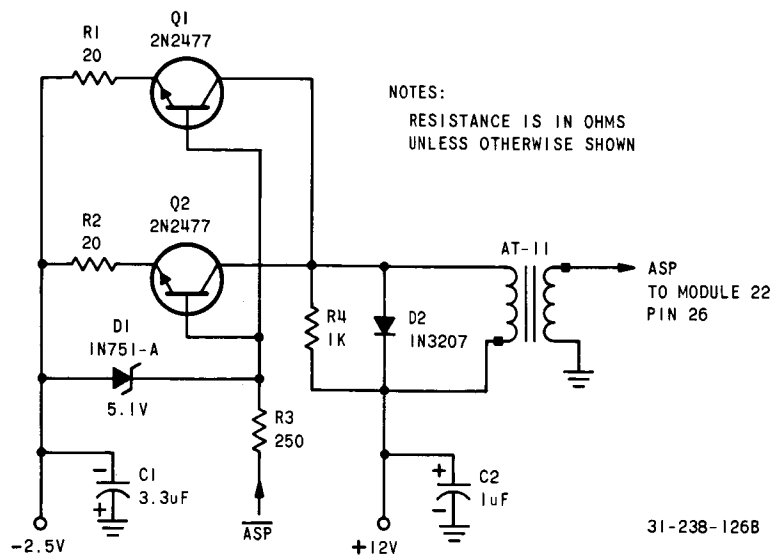
Figure II-27. Word-Current Base Regulator
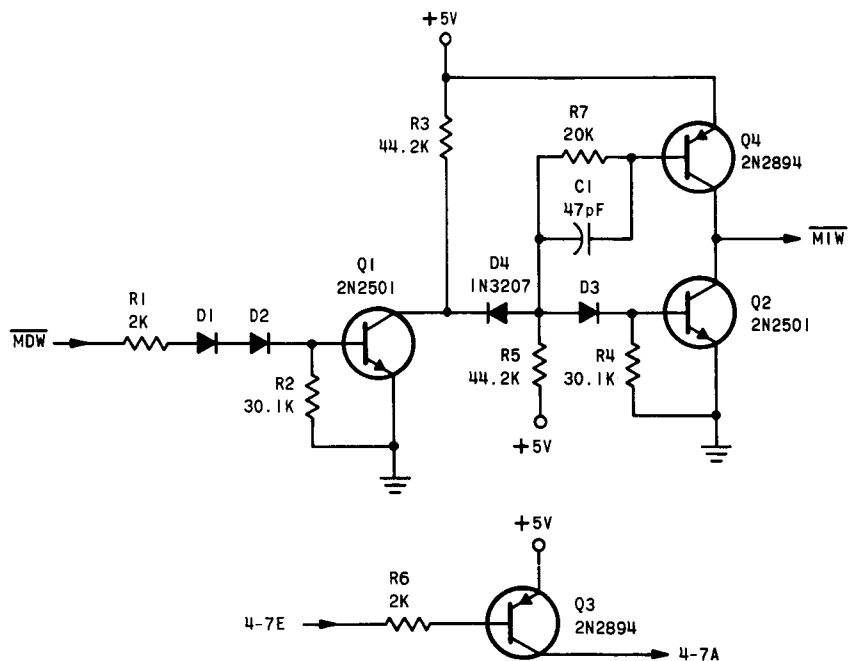
Figure II-28. Clock Amplifier and
Data Input Preamplifier
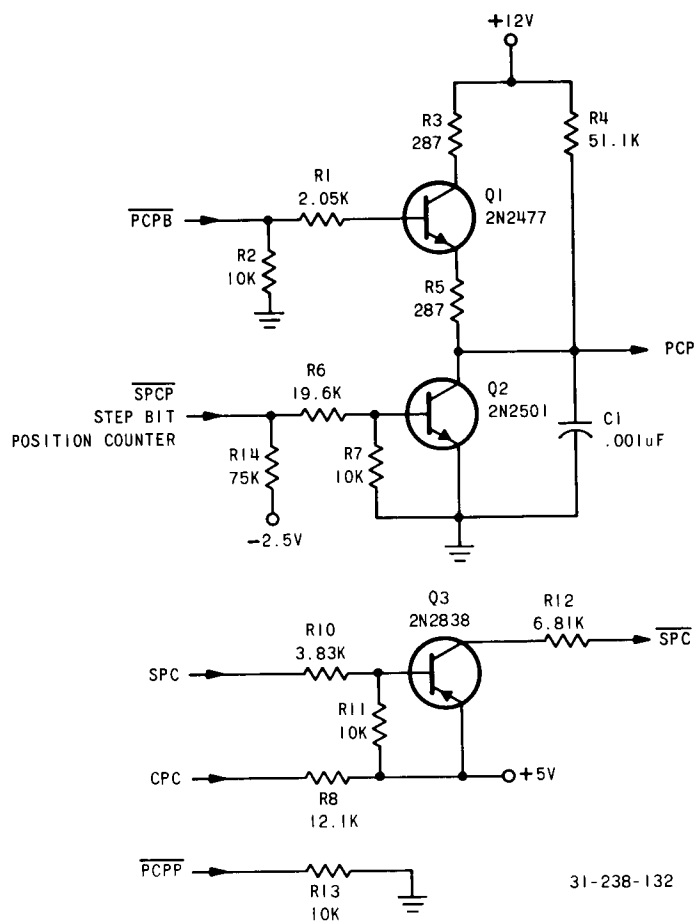
NOTES:
DIODE ARE TYPE MC456 UNLESS
OTHERWISE SHOWN

Figure II-29. Bit-Position-Counter Gate

NOTE:
RESISTANCE IS IN OHMS UNLESS OTHERWISE SHOWN.
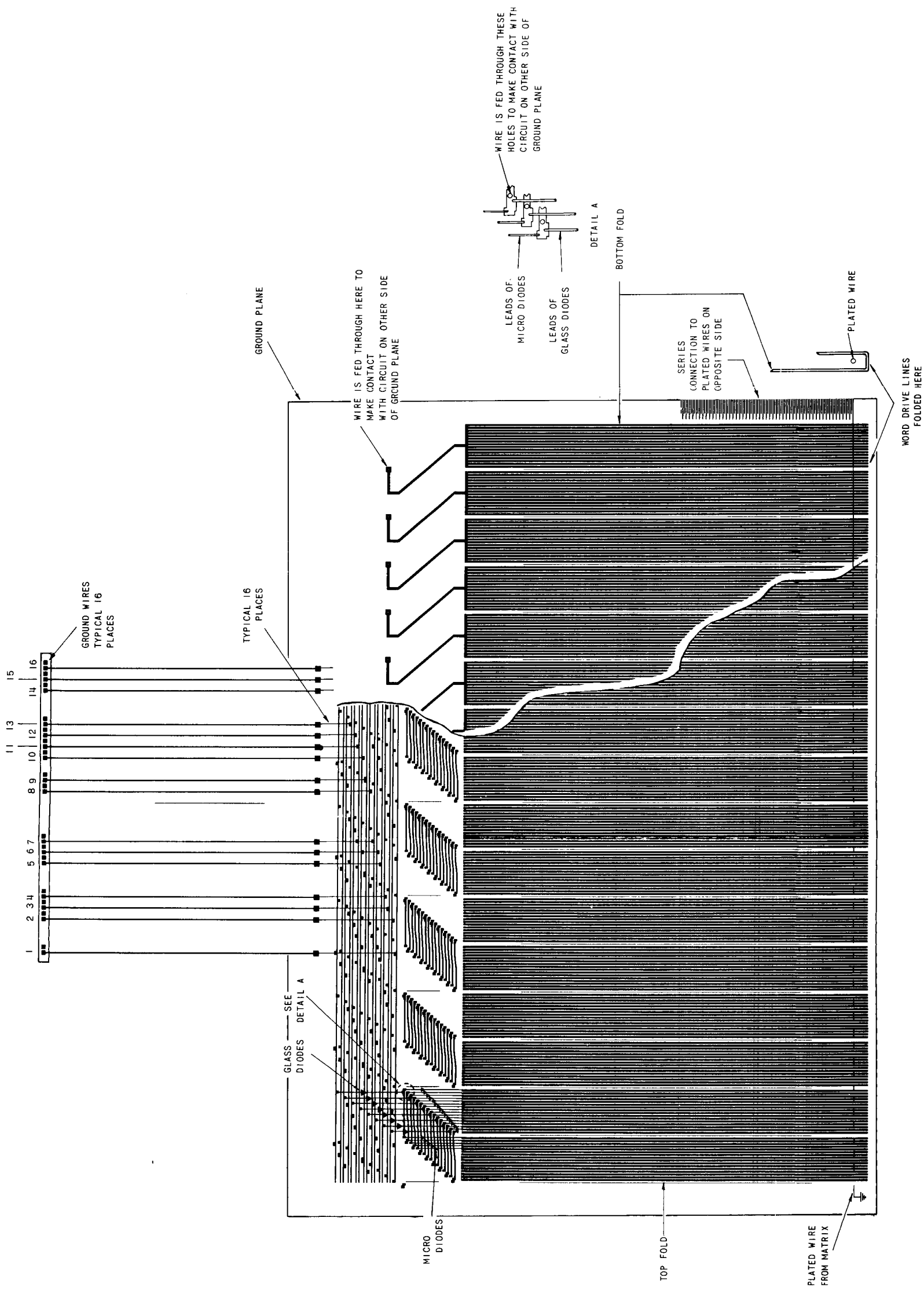
Figure III-1. Aerospace Memory Plane, Top View

APPENDIX III

The layout of the memory plane and of the multilaminate backboards are contained in this appendix.
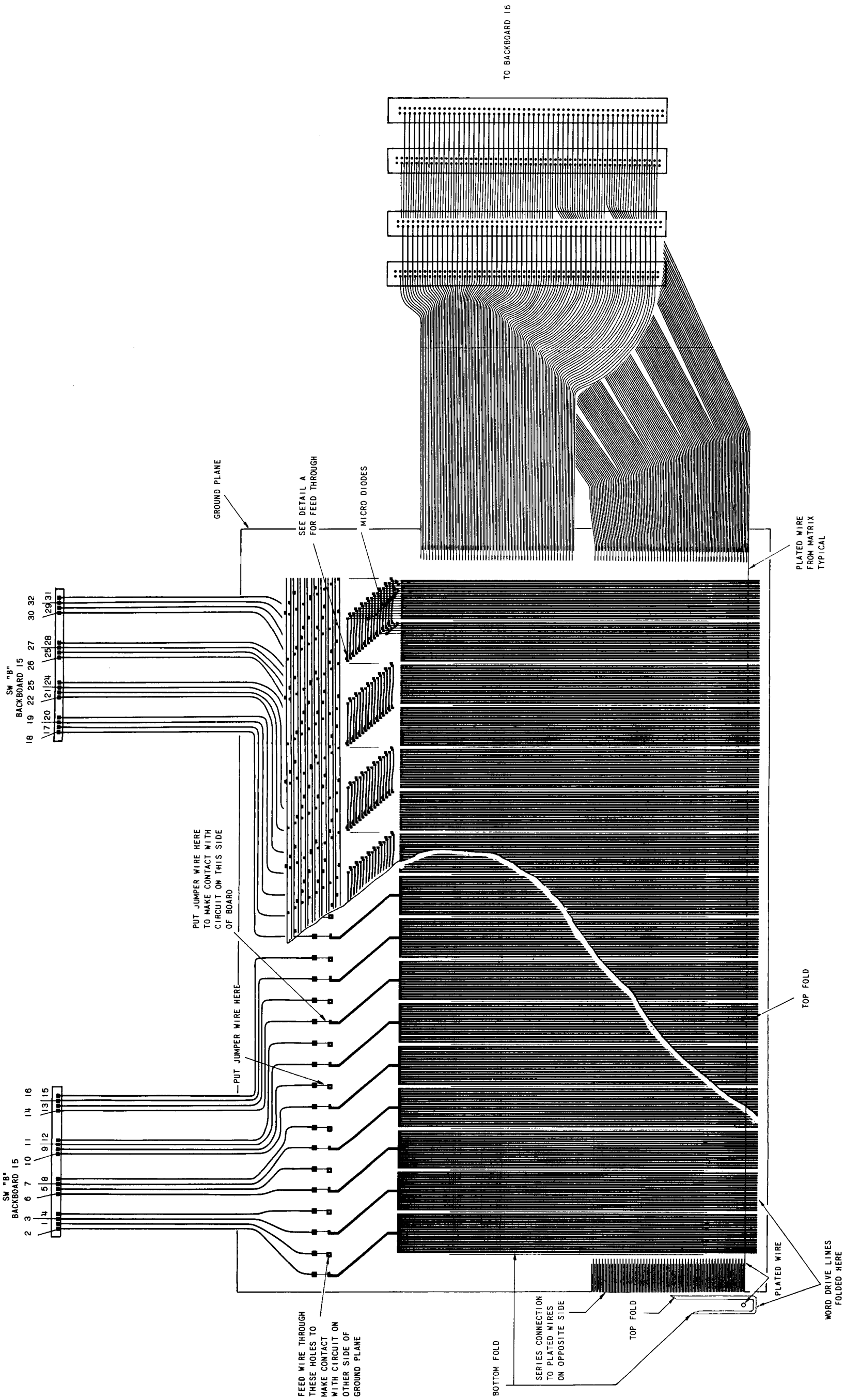
Figure III-2. Aerospace Memory Plane, Bottom View
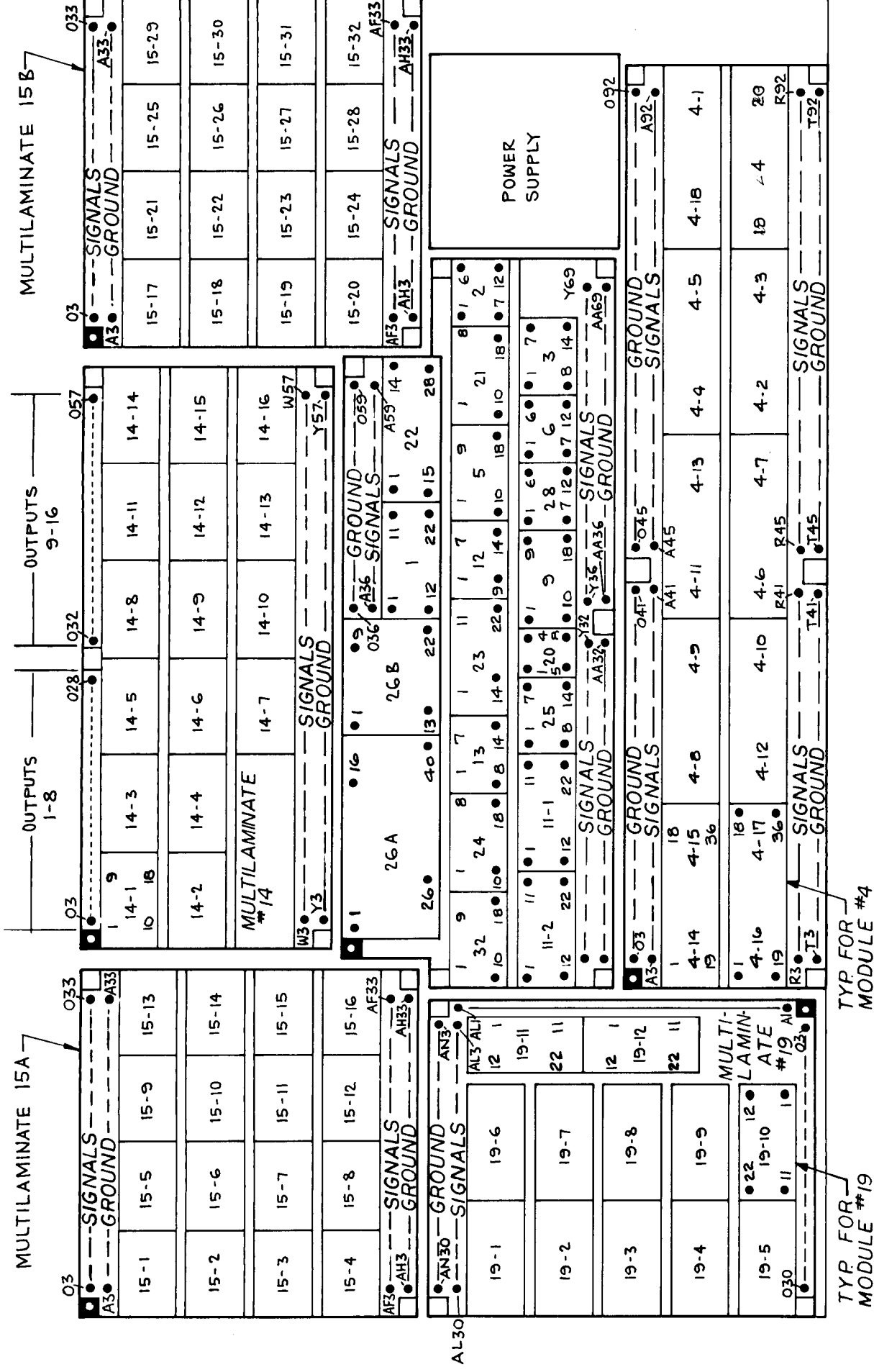
III-5/III-6

Figure III-3. Wiring Side Multilaminate A, Backboard View
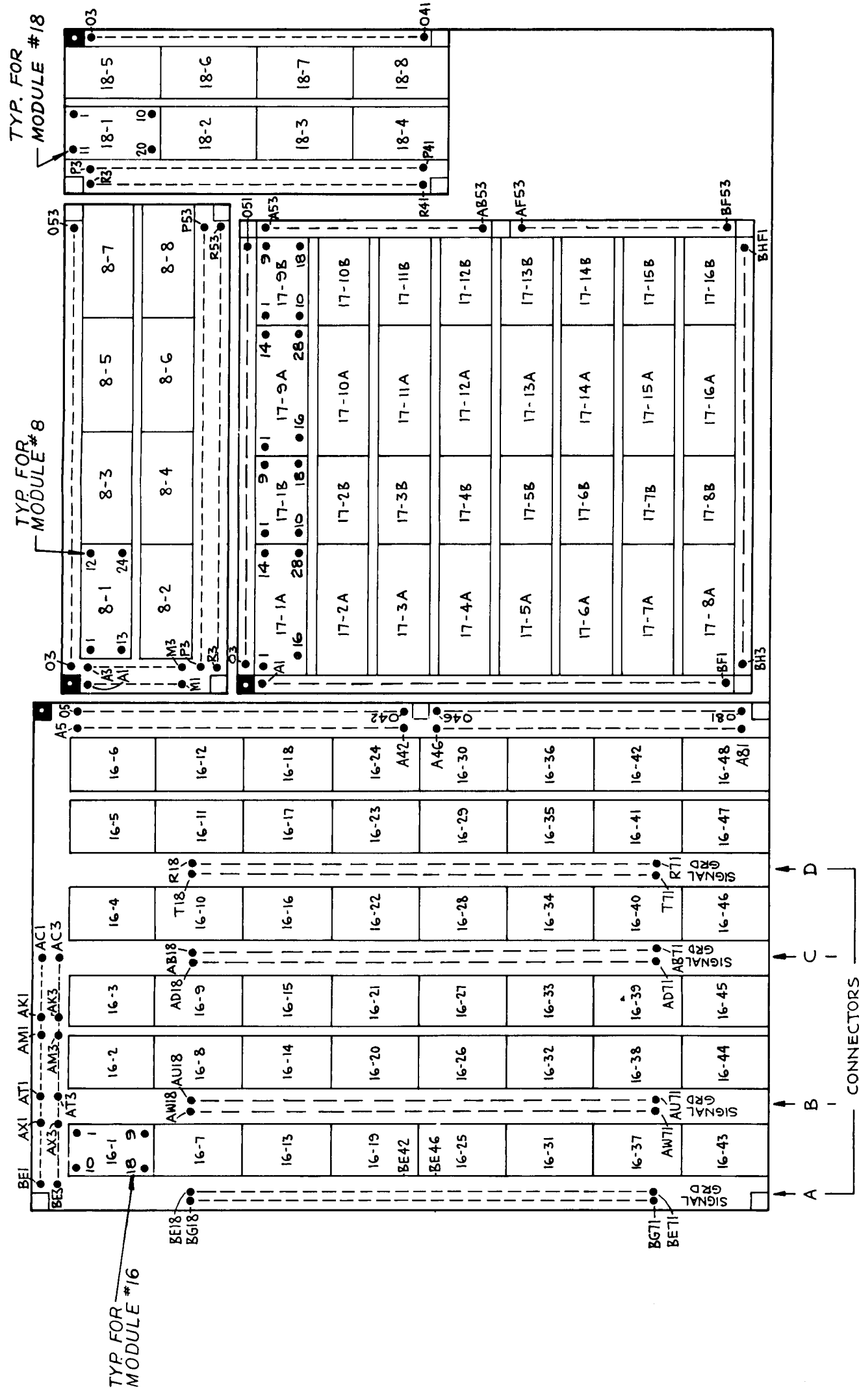
Figure III-4. Wiring Side Multilaminate
B, Backboard View

APPENDIX IV

A brief statement concerning the reliability of plated-wire memories built to date is contained in this appendix.

RELIABILITY HISTORY OF MEMORY SYSTEM AND MEMORY PLANE

During final testing of the breadboard memory model, the breadboard was operated continuously for 480 hours with the memory plane at +70°C to +75°C. The only errors that were made during this period were associated with the laboratory starting time and stopping time. These errors were caused by large transients in the power mains. No attempt was made to eliminate these errors because the very temporary nature of the model wiring and the use of unregulated laboratory power supplies would not have permitted significant information to be obtained.

An experimental plated-wire memory plane containing 32 words of ten bits each was tested after accelerated aging. It was stored for 1675 hours at +90°C and 95 percent relative humidity. The glass-epoxy etched-circuit laminates were noticeably discolored, and the blue polyurethane insulation started to lose its luster. All the bits in the plane were still in good operating condition. The prevision of the measurements and the lack of exact repeatability of the drive current waveforms make it impossible to say that there were no changes. If there were any changes, no trend was discernible, and the changes were less than the combined accuracy and repeatability of the measurement, about 15 percent. For a detailed discussion of reliability history of resistors and capacitors, refer to monthly report No. 9.

APPENDIX V

PLATED-WIRE SPECIFICATION PW-4A

Scope: This specification is for plated wire that will be used in planes for the Goddard Memory.

Mechanical: The wire shall be supplied in lengths of 18 inches ±1/2 inch. The wire shall be free of kinks and bends and nominally five mils in diameter. The d-c resistance of the wire shall be 1.5 Ω/foot ±5 percent.

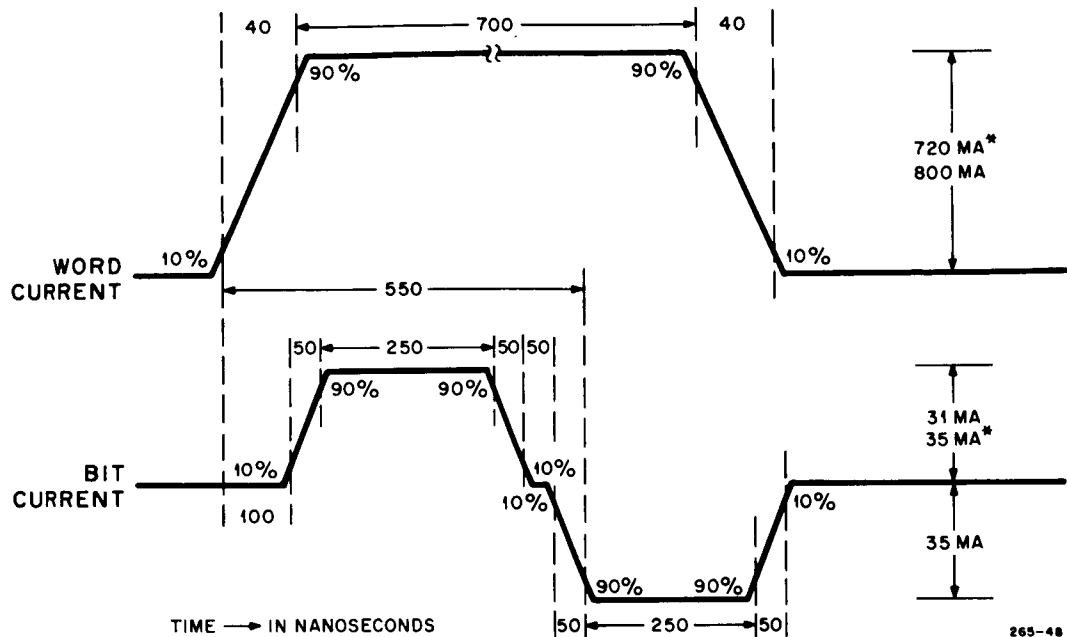Electrical: The following program shall be applied to the wire.

265-47
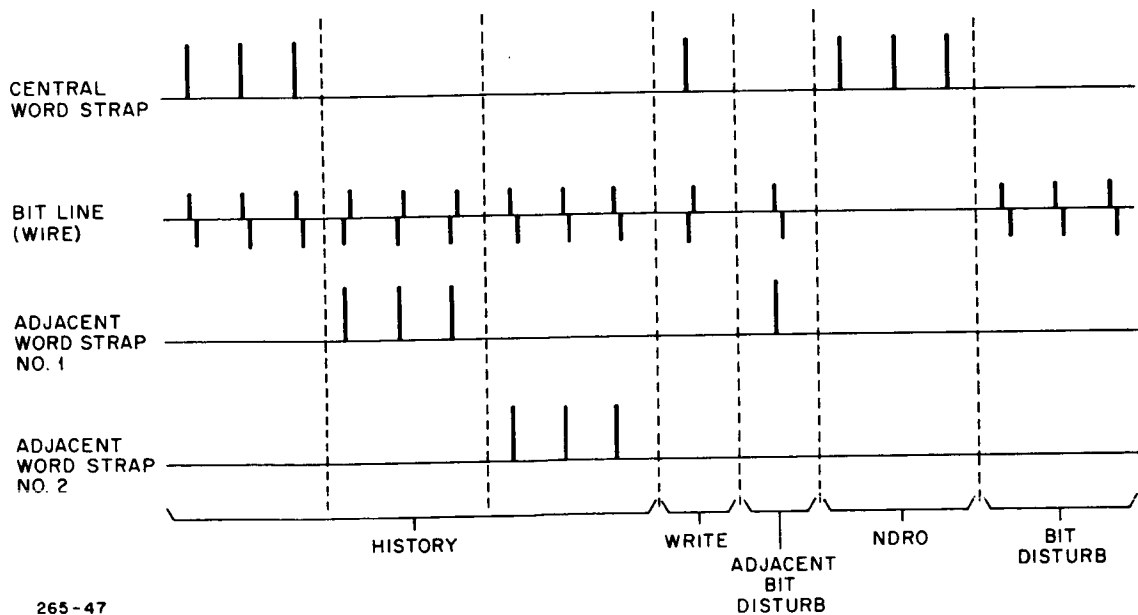
(On next half cycle, pattern repeats with opposite polarity of bit current.)

The detailed character of the pulses shall be:

    a. History phase

        Twenty pulses of word current suitably overlapped with bipolar bit
pulse will be used.

        In addition to the history phase on the central word strap, a his-
tory phase is applied to the two immediately adjacent straps. For the strap
ultimately to be exercised by the ABD current, the bit polarity was such as
to store the opposite information as stored under the control word strap dur-
ing the history phase in the other adjacent strap; in the other adjacent
strap the bit polarity is such as to store the same information as stored
under the central word strap during the history phase.

    b. Write phase

        Only one word pulse and overlapped bipolar bit writing current shall
be used.
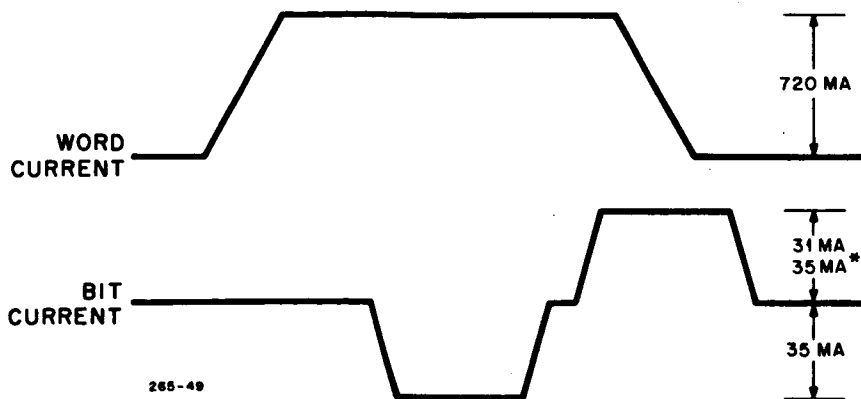
WORD CURRENT

720 MA

BIT CURRENT

31 MA
35 MA*

35 MA

265-49

NOTE:

*The asterisked values will be used in initial testing due to equipment limitation.

Nonasterisked values will be used when more versatile equipment is available.

c. Adjacent bit disturb

One word pulse will be applied with suitably overlapping bit pulses.

WORD CURRENT

800 MA

BIT CURRENT

31 MA
35 MA

35 MA

265-50
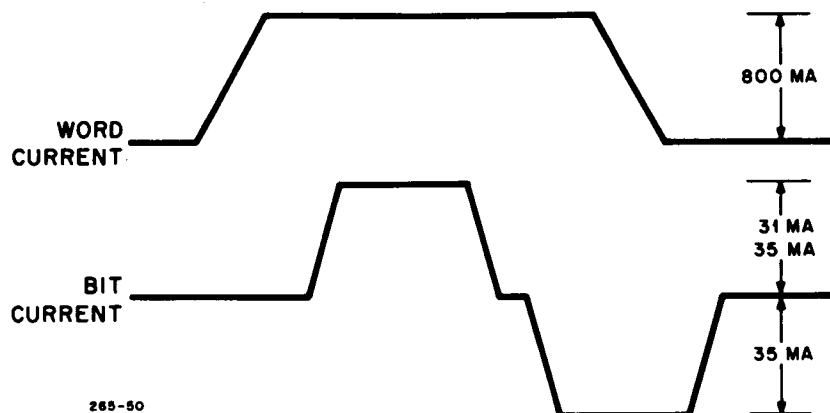
d. NDRO phase

Two hundred word current pulses of the following nature will be applied.

800 MA

265-51

e. Bit disturb

Fourty bipolar bit disturbs will be applied.
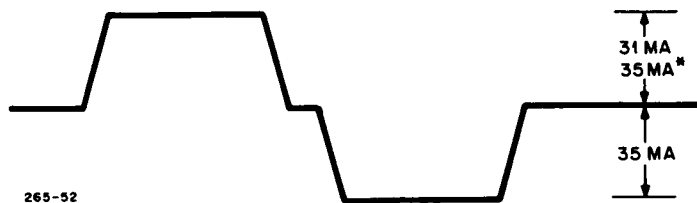
265-52

NOTE:

*The asterisked values will be used in initial
testing due to equipment limitation.

Nonasterisked values will be used when more
versatile equipment is available.

Under this regime of pulses, the read output due to the first word
current pulse in the history phase shall be seven millivolts for a negative
output and three millivolts for a positive output with the following arrange-
ment of word strap and wire.

265-53
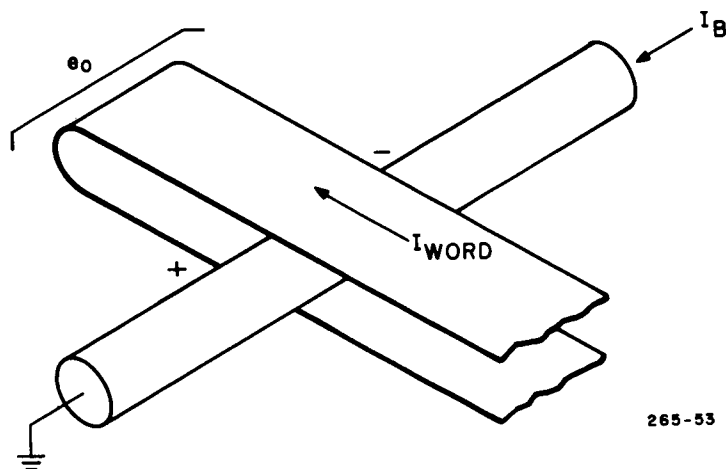
Additional Requirements: The read output shall not change more than one
millivolt when the wire is subjected to a tensile
force of 20 grams or an angular twist of 22.5^o
(clockwise or counterclockwise) applied either
separately or together. This will be on a
sampling basis.

The bit disturb pulse shall be made unipolar in
the bit distrub slot and increased so that it di-
minishes the read output 25 percent. The value of

V-4

bit current at which this occurs will be greater than ±50 milliamperes. The test will be repeated for both polarities of the disturbing bit current. In performing this test, a multiple write operation is used with a unipolar bit pulse to allow for observation of a sharper threshold. This test is performed on a sampling basis. The NDRO pulses are also increased (on a sample basis) until the read output decreases 25 percent. The minimum current at which this decrease obtains shall be 820 milliamperes for the positive output pulse and 920 milliamperes for the negative output pulse.

All tests shall be conducted using a 35-mil wrap-around everywhere-equidistant word-strap overlay with a 50-mil center-to-center spacing. The distance between the two halves of the word strap shall be ten mils.

APPENDIX VI

The power supply specification and test data are given in Appendix VI.

Aerospace DC to DC Converter - Requirements

1. Normal Input   +28 VDC.   +5.5V   Maximum input power for +28V input is 300 milliwatts for all load and ambient temperature variations.

2. Abnormal Input   +40V continuous
                   +70V for 10 millisecond transient

   Output voltages must not exceed 125% of nominal voltages for all abnormal input conditions.

   No damage will be caused by abnormal input.

   The negative connection for the 28V input may be the common output terminal.

3. Output Voltages, Currents: The listed nominal voltages must be obtained within ±1% at 25°C; 28V input; maximum stated current in the three loads.

+12V.DC	7 ma. max.	3.5 ma. min.
+5V.DC	15 ma. max.	7.5 ma. min.
-2.5V.DC	2 ma. max.	0.9 ma. min.

   No damage will be caused by accidental short circuit or open circuit of the load.

   The three output voltages may have one common terminal.

4. Regulation and Stability: The output voltages specified should be maintained within ±2% for all combinations of stability, static variation of normal input voltage, static variation of specified output currents and slowly changing temperature. Regulation shall be accomplished by the "Pulse Width" technique. The intent of this requirement is to make conversion losses as independent of normal input variations as is possible.

5. Ripple: Less then ±2.5 mv for normal input.

6. Environmental Conditions:

Ambient Temperature	-20°C to +50°C
Relative Humidity	100% max.
Altitude	Sea level to deep space vacuum.

Important Design Objectives:

7. Minimum conversion losses, 65 milliwatts, for all normal input conditions and any load in specified range.

8. Physical Size: Three cubic inches or less. One dimension should be 0.8 inch or less.

9. Weight: Four ounces or less - may go over.

10. Vibration: Fifteen "g" peak sine wave vibration over a frequency range of 5 cps to 3 kcs.

Table VI-1.   Power Supply Data for Interelectronics Supply, Serial No. 236671

LOADS	+12 VOLT OUTPUT			+5 VOLT OUTPUT			-2.5 VOLT OUTPUT			INPUT VOLTAGE (V) AND INPUT CURRENT (MA)
	-20°C	+25°C	+50°C	-20°C	+25°C	+50°C	-20°C	+25°C	+50°C	
FULL LOAD: +12V 1.715K		11.99 11.98 12.00			5.000 4.993 5.014			-2.480 -2.481 -2.480		+25°C 28.00V @ 9.8 ma 23.50V @ 11.6 ma 33.50V @ 8.6 ma
+5V 333Ω -2.5V 1.250K	12.28 12.29 12.27			2.505 2.449 2.355			-0.657 -0.575 -0.560			-20°C 28.00V @ 6.5 ma 33.50V @ 5.8 ma 23.50V @ 7.2 ma
			11.83 11.82 11.85			4.92 4.92 4.92			-2.37 -2.37 -2.38	+50°C 28.00V @ 9.5 ma 23.50V @ 11.7 ma 33.50V @ 7.8/9.0
HALF LOAD: +12V 3.430K		11.99 11.98 12.01			5.075 5.075 5.076			-2.490 -2.490 -2.490		+25°C 28.00V @ 5.6 ma 23.50V @ 6.4 ma 33.50V @ 5.2 ma
+5V 666Ω -2.5V 2.780K	12.28 12.29 12.28			+3.803 3.753 3.481			-1.880 -1.820 -1.636			-20°C 28.00V @ 4.8 ma 33.50V @ 4.4 ma 23.50V @ 4.9 ma
			11.83 11.81 11.88			4.97 4.95 4.95			-2.38 -2.38 -2.36	+50°C 28.00V @ 5.7 ma 23.50V @ 6.2 ma 33.50V @ 5.2 ma

RIPPLE MEASURED WITH +24V INPUT AND FULL LOAD ON OUTPUT	+12 VOLT	+5 VOLT	-2.5 VOLT
	15 millivolts p-p 200 cycles	6 millivolts p-p 2 kilocycles	Stable

APPENDIX VII

This appendix contains photographs of oscilloscope waveforms of various signals in the memory unit. These photographs are presented as an aid to understanding the operation of the system and as an aid for troubleshooting malfunctions. All positive signals are upward except where noted.
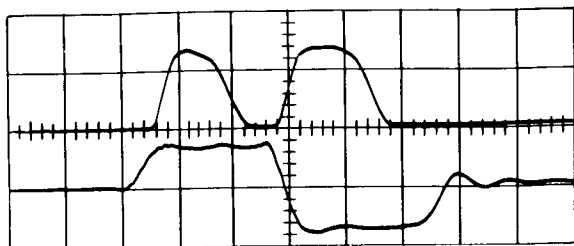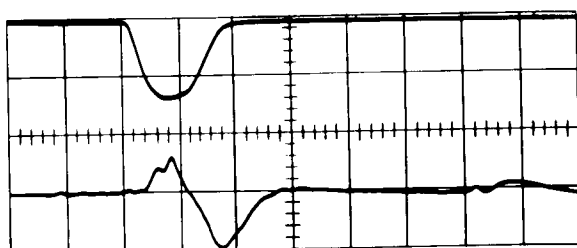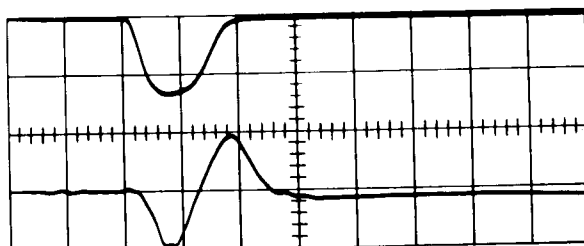
a. Writing a "Zero"
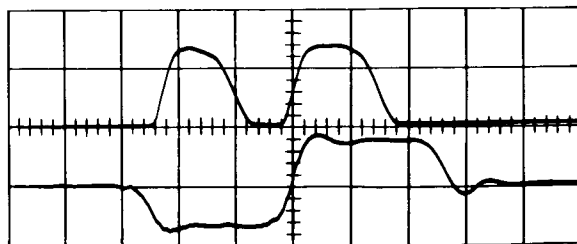
b. Writing a "One"
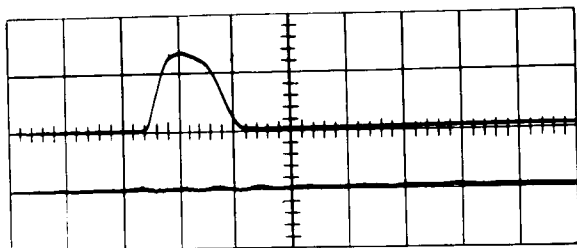
RECORDED AT:
    0.2 μSEC/DIV. (HORIZONTAL)
UPPER TRACE
    500 MA/DIV. – WORD CURRENT (VERTICAL)
LOWER TRACE
    50 MA/DIV. – BIT CURRENT (VERTICAL)

c. Reading

Figure VII-1.   Word Current in Selected Word Line (Upper Trace)
and Bit Current in Plated Wire (Lower Trace)

a. Readout of Stored "One"

b. Readout of Stored "Zero"

READOUT SIGNAL RECORDED AT:
    0.2 μSEC/DIV. (HORIZONTAL)
    0.2 VOLTS/DIV. (VERTICAL)

Figure VII-2.   Collector of First Stage of Sense Amplifier During Readout of
Plated Wire (Upper Trace) and Word Current (Lower Trace)
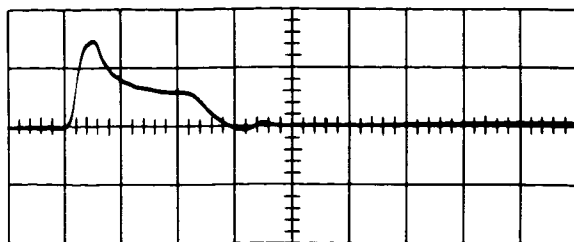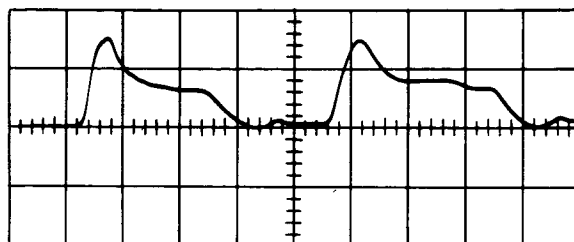
a. Read   b. Write

RECORDED AT:
0.1μSEC/DIV. (HORIZONTAL)
5 VOLTS/DIV. (VERTICAL)

Figure VII-3.   Output of A-Switch
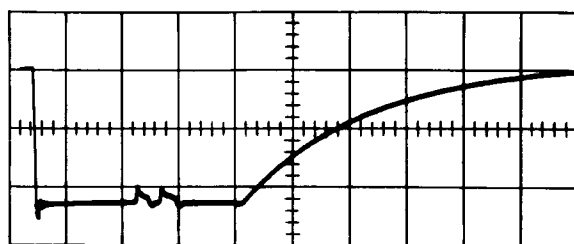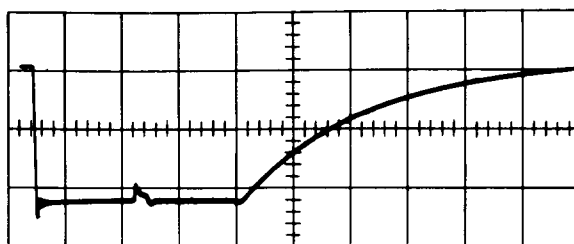
a. Write   b. Read

RECORDED AT:
1.0 μSEC/DIV. (HORIZONTAL)
5 VOLTS/DIV. (VERTICAL)

Figure VII-4.   Output of B-Switch
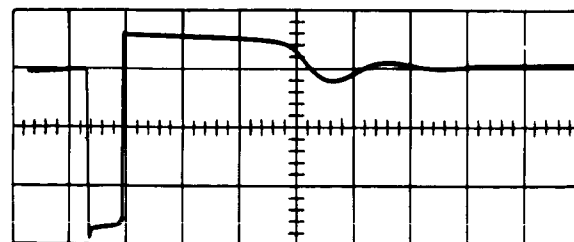
RECORDED AT:
2.0 μSEC/DIV. (HORIZONTAL)
2 VOLTS/DIV. (VERTICAL)

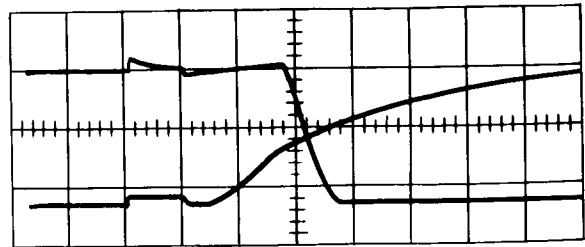Figure VII-5.   Output of Blocking
Oscillator for Stored "One"
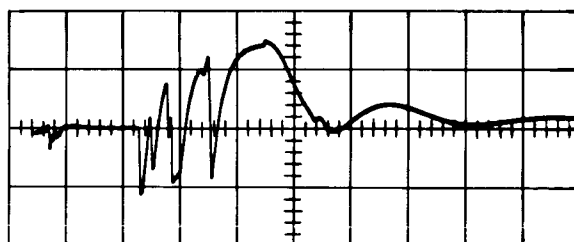
RECORDED AT:
1.0 μSEC/DIV. (HORIZONTAL)
1 VOLT/DIV. (VERTICAL)

Figure VII-6.   Collector of First
Stage of Sense Amplifier Showing
Overload Due to Bit Transient
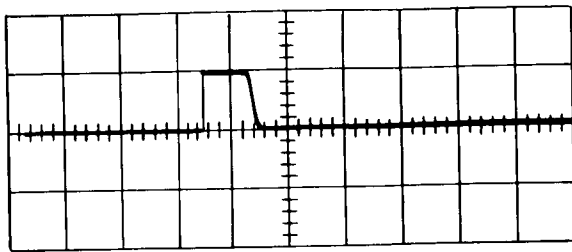
RECORDED AT:
5 μSEC / DIV. (HORIZONTAL)
5VOLTS/DIV. (VERTICAL)

Figure VII-7. Step Pulse Which Causes Action (a.) and
Stepping Action of P-, B-, or A-Counter (b.)
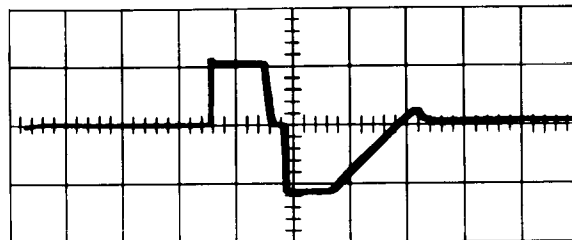
RECORDED AT:
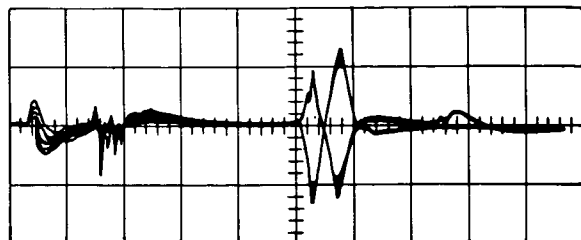5 μSEC / DIV. (HORIZONTAL)
1 VOLTS/DIV. (VERTICAL)

Figure VII-8. Common Anode Line of P-, B-, or
A-Counter Showing Power Pulse Which Places Counter
in High Conduction State Followed by the Dropping
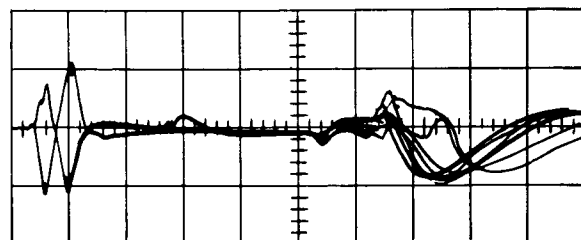of the Potential of the Common Anode Due to
Step Pulse
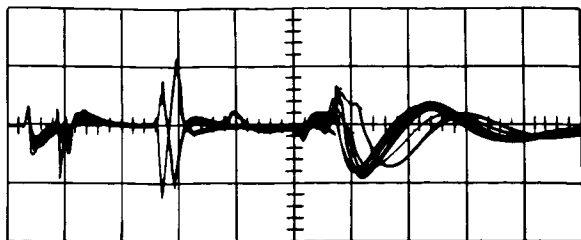
a. SHOWS NOISE DUE TO THE MATRIX AND
B-SWITCH TURNING ON FOLLOWED BY
PLATED WIRE OUTPUTS WHICH ARE
FOLLOWED BY NOISE DUE TO MATRIX
TURNING OFF.

b. SHOWS FIRST HALF OF WAVEFORM a.
EXPANDED.

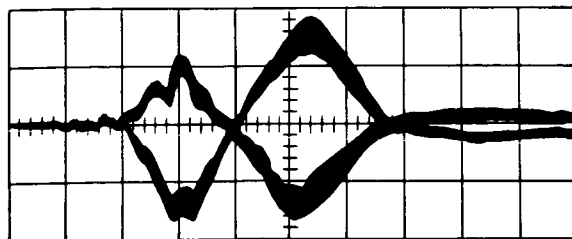c. SHOWS SECOND HALF OF WAVEFORM a.
EXPANDED.

WAVEFORM a. RECORDED AT:
1.0 μSEC/DIV. (HORIZONTAL)
0.2 VOLTS/DIV. (VERTICAL)

WAVEFORMS b.& c. RECORDED AT:
0.5 μSEC/DIV. (HORIZONTAL)
0.2 VOLTS/DIV. (VERTICAL)

Figure VII-9. Collector of TR1 of Sense Amplifier with the Output of
512 Word Locations on Each of 12 Plated Wires Superimposed

RECORDED AT:
100 nSEC/DIV.(HORIZONTAL)
0.2 VOLTS/DIV.(VERTICAL)

Figure VII-10. Collector of TR1 of
Sense Amplifier Showing Plated-Wire
Outputs of 1/16 of Entire Memory, or
6144 Bits, Superimposed

This appendix contains specifications applicable to the transistors, diodes, resistors, capacitors, and transformers used in the memory. Also presented are the end-of-life factors used for circuit design component derating.

TRANSISTORS

		Minimum	Maximum
2N2501 NPN	V_{BE} @ I_b = 20 μa, I_c = 200 μa		0.7 v
	V_{CE} @ I_b = 20 μa, I_c = 200 μa		0.25 v
Motorola*	V_{BE} @ I_b = 10 ma, I_c = 100 ma		1.05 v
	V_{CE} @ I_b = 10 ma, I_c = 100 ma		0.35 v
	H_{FE} @ I_c = 100 ma, V_{CE} = 0.4 v	30	
	H_{FE} @ I_c = 600 μa, V_{CE} = 0.3 v	30	
	I_{EBO} @ V_{EBO} = +7 volts, 100°C		0.1 μa
	I_{CER} @ V_C = 12 volts, R_{BE} = 100 kΩ, 100°C		1.0 μa
2N2894 PNP	V_{BE} @ I_b = 1 ma, I_c = 10 ma		0.9 v
	V_{CE} @ I_b = 1 ma, I_c = 10 ma		0.1 v
Fairchild*	V_{BE} @ I_b = 6 ma, I_c = 60 ma		0.14 v
	V_{CE} @ I_b = 6 ma, I_c = 60 ma		0.21 v
	H_{FE} @ I_b = 50 μa, V_{CE} = 0.3 v	30	
	H_{FE} @ I_b = 1 ma, V_{CE} = 0.15 v	20	
	H_{FE} @ I_b = 6 ma, V_{CE} = 0.45 v	20	
	I_{CER} @ V_C = 10 volts, R_B = 100 kΩ, 100°C		0.1 μa

*Manufacturer

		Minimum	Maximum

2N2838
PNP

Fairchild*

V_{BE} @ I_b = 15 ma, I_c = 150 ma — 1.1 v

V_{CE} @ I_b = 15 ma, I_c = 150 ma — 0.3 v

V_{BE} @ I_b = 20 μa, I_c = 200 μa — 0.6 v

V_{CE} @ I_b = 20 μa, I_c = 200 μa — 0.2 v

H_{FE} @ I_c = 150 ma, V_{CE} = 0.4 v 30

H_{FE} @ I_c = 200 μa, V_{CE} = 0.3 v 30

I_{CER} @ V_{CE} = 12 volts, R_B = 100 kΩ, 100°C — 1.0 μa

I_{EBO} @ V_{EBO} = 5 volts, 100°C — 3.0 μa

2N918 (Amplifier Gate Transistor)
NPN

Fairchild*

H_{FE} @ I_c = 30 ma, V_{CE} = 1.0 v 20

I_{cbo} @ V_{cb} = 10 volts — 10 na

C_{ob} @ V_{cb} = 10 volts — 1.7 pf

V_{cb} @ I_b = 1 ma, I_E = 0 0.70 v 0.79 v

V_{OE} @ I_b = 1 ma, I_E = 0 — 2 mv

r_s @ I_b = 1 ma, I_E = 0 — 50 Ω

T_s @ I_b = 1 ma, I_{b2} = 5 ma — 30 ns

2N918 (Blocking Oscillator)
NPN

Fairchild*

H_{FE} @ I_c = 13 μa, V_{CE} = 5 v 4 9

H_{FE} @ I_c = 10 ma, V_{CE} = 0.25 v 20

I_{cbo} @ V_{cb} = 10 volts — 10 ma

V_{Eb} @ I_E = 12 μa, V_{cb} = 5 v 0.57 v 0.61 v

V_{Eb} @ I_E = 10 ma, V_{cb} = 0 70 v 81 v

H_{FE} @ f = 100 mc, I_c = 4 ma, V_{CE} = 10 v 6

h_{ib} @ I_c = 13 μa, V_{CE} = 5 v, f = 350 kc 2 kΩ

C_{ob} @ I_E = 0, V_{cb} = 10 v 2 pf

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* Manufacturer

	Minimum	Maximum

2N995 or **2N3012**
PNP

Fairchild*

	Minimum	Maximum
H_{FE} @ I_c = 25 ma, V_{CE} = 0.25 v	25	
V_{be} @ I_b = 2 ma, I_c = 0	0.77 v	0.91 v
V_{CE} @ I_c = 25 ma, I_b = 2 ma		0.2 v
V_{OE} @ I_b = 2 ma, I_E = 0		2.5 mv
r_s @ I_b = 2 ma, I_E = 0		25 Ω

2N2477
NPN

RCA*

	Minimum	Maximum
H_{FE} @ I_c = 860 ma, V_{CE} = 1.1	16	
V_{CE} @ I_c = 860 ma, I_b = 110 ma	0.7 v	0.9 v
V_{be} @ I_c = 860 ma, I_b = 110 ma	1.2 v	1.6 v

2N709A
NPN

Sylvania*

	Minimum	Maximum
I_{cbo} @ V_{cbo} = 2 v, 100°C		0.5 μa
H_{FE} @ I_c = 100 μa, V_{CE} = 2 v	25	85
V_{bE} @ I_c = 100 μa, V_{CE} = 2 v	0.58 v	0.65 v
C_{ob} @ f = 1 mc, V_{cb} = 0.2 v, I_E = 100 μa		3 pf
H_{FE} @ f = 20 mc, V_{CE} = 2 v, I_C = 100 μa	4	
h_{ib} @ I_c = 100 μa, V_{cb} = 2.5 v, f = 50 k		250 Ω

DIODES

1N3207

Microsemi-
  conductor*

1. Word line diode

	Minimum	Maximum
V_f @ 800 ma plateau	1.1 v	1.3 v
I_r @ V_r = 24 v @ 100°C		3 μa

2. Logic diode

	Minimum	Maximum
V_f @ 1 ma		0.60 v
I_r @ V_r = 24 v @ 100°C		3 μa

MC456

Microsemi-
  conductor*

	Minimum	Maximum
V_f @ 0.5 μa	0.35 v	
V_f @ 45 μa		0.56 v

*Manufacturer

RESISTORS AND CAPACITORS

Resistors

Manufacturer	Type	Tolerance	Temp. Coeff.	Wattage
Daven	DA4B	±1%	+360 ppm/±°C	1/4
Electra	MF4CT2	±1%	±50 ppm/±°C	1/10
ACI	CE 1/4	±1%	±100 ppm/±°C	1/4
T.I.	TM 1/8	±10%	+0.7%/°C	1/8

Capacitors

Manufacturer	Type	Tolerance	Obtainable Capacitance
Corning	CYFM-10	±5%	1 to 300 pf
Vitramon	VK 20	-10 or 20%	10 to 1000 pf
	VK 30	-10 or 20%	1200 to 10,000 pf
Components, Inc.	Series T	+20 or 40%	0.22 to 4.0 mf
Sprague	150D	±10%	0.22 to 6.8 μf, case size A 6 volts

TRANSFORMERS

AT1

Core Material - Indiana General T1

Core Size - CF-101
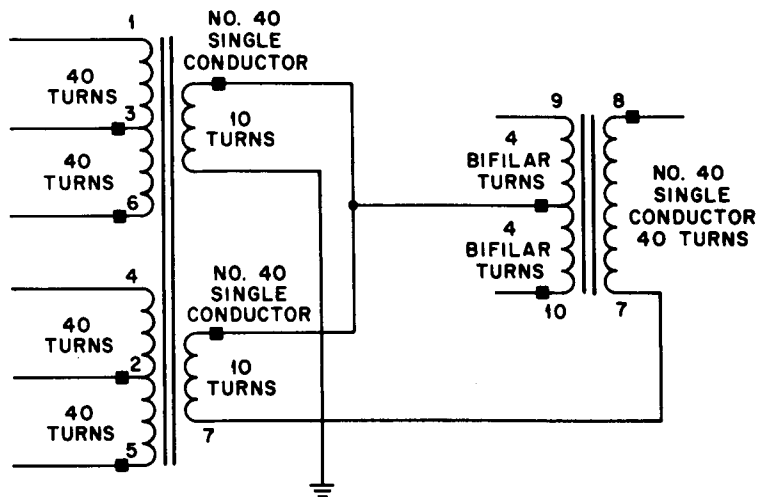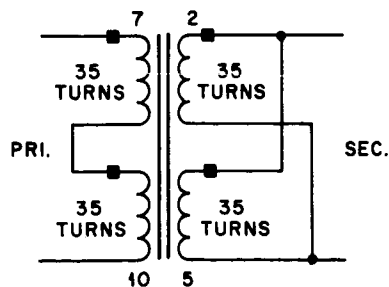
Wire Size - No. 38 Bifilar
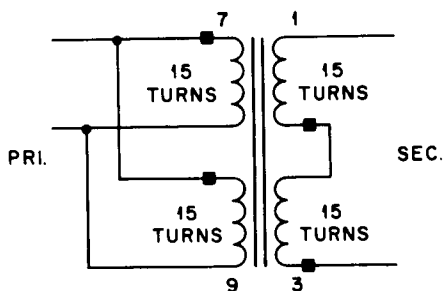
AT2   Core Material – Indiana General T1

Core Size – CF-101

Wire Size – No. 38 Bifilar
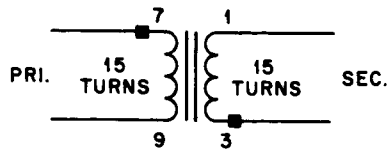
AT3   Core Material – Indiana General T1

Core Size – Both cores CF-102

Wire Size – As shown
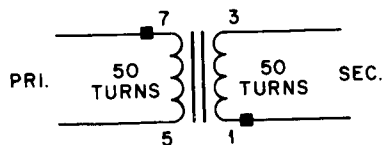

AT4   Core Material – Indiana General T1

Core Size – CF-101

Wire Size – No. 40 Bifilar

AT5 and AT6   Not Used

AT7　　　　　　　Core Material – Indiana General T1

Core Size – CF-101

Wire Size – No. 38 single conductor
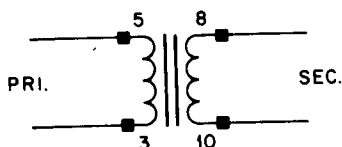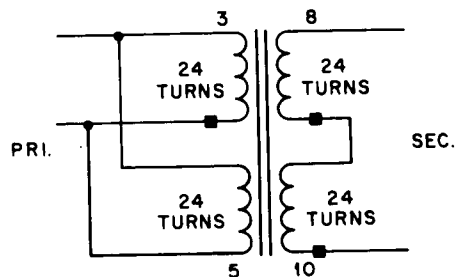

AT8　　　　　　　　　　Not Used

AT9　　　　　　　Core Material – Indiana General T1

Core Size – CF-101

Wire Size – No. 40 Bifilar

Winding consists of 3 feet 9 inches
of No. 40 Bifilar, minimum induc-
tance, 3.8-millihenry winding
wound in three layers.

AT10　　　　　　Core Material – Indiana General T1
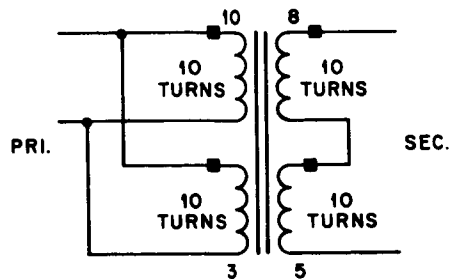
Core Size – CF-102

Wire Size – No. 38 Bifilar

AT11   Core Material – Indiana General T1

       Core Size – CF-102

       Wire Size – No. 38 Bifilar

END-OF-LIFE (E.O.L.) FACTORS FOR CIRCUIT DESIGN COMPONENT DERATING

The initial component specification is multiplied by the appropriate E.O.L. factor to give the E.O.L. value of the parameter in question. For example:

    Transistor beta specification

    H_{FE} @ I_c = 10 ma, V_{ce} = 2 v   30 min

    End of life H_{FE} = 30 × 0.4 = 12

    End of life V_{ce} = 0.2 v × 1.3 v = 0.26 v

Therefore, the circuit using this transistor must work with a transistor whose beta is a maximum of 12 and whose V_{ce} is a minimum of 0.26 volt.